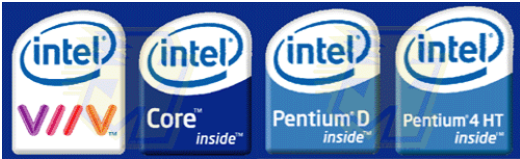


# MS-7356 Ver : 10

Intel (R) LGA775 Processor  
Intel (R) Bearlake ( GMCH ) + ICH9/ICH9R Chipset



- CPU:**
- Intel - Conroe 2.66G (E6700)
  - Intel - Presler 3.73G (PentiumEE965)
  - Intel - SmithField 3.2G (Pentium EE840)
  - Intel - Kentsfield
  - Intel - Prescott 3.73G (P4-EE-3.73GHz)
  - Intel - CedarMill 3.73G (Celeron D356)
  - Intel - Gallatin 3.46G (P4-EE-3.46GHz)
  - Intel - Yorkfield

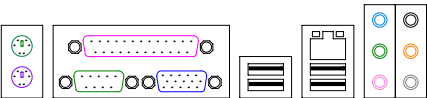
- System Chipset:**
- Intel Bearlake P35/G33 (North Bridge) Rev : A2
  - Intel ICH9 / ICH9R (South Bridge) Rev : A2

- On Board Chipset:**
- CLOCK : ICS9LPRS906CG
  - LAN : RTL8111B
  - IEEE1394a : VT6308
  - IDE Bridge : Marvel 88SE6111
  - LPC Super I/O : F71882FG
  - Audio Codec : ALC888 7.1 Channel Ver : A1
  - BIOS : SPI- 8M

- Main Memory:**
- Dual-channel DDR III \* 4 (Max 4GB)

- Expansion Slots:**
- PCI EXPRESS X16 SLOT \* 1
  - PCI EXPRESS X4 SLOT \* 1 Alternative
  - PCI EXPRESS X2 SLOT \* 2 Alternative
  - PCI 2.2 SLOT \* 2

ATX Size 305mm \* 244mm(OSP)

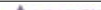


RoHS

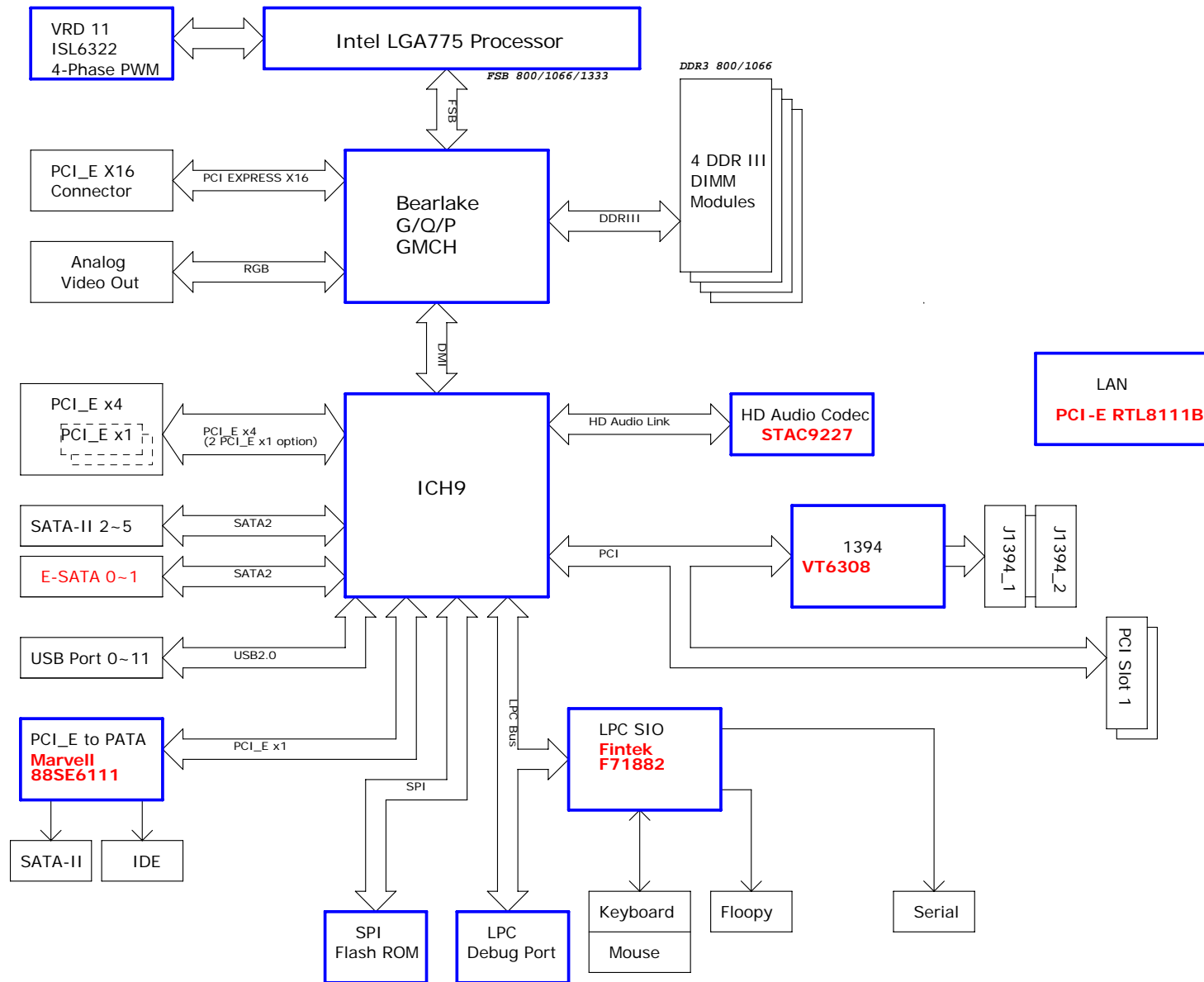
1	Cover Sheet
2	Block Diagram
3	Clock Generate - ICS9LPRS906
4	Intel LGA775 - Signals
5	Intel LGA775 - Power
6	Intel LGA775 - GND
7	Intel Bearlake - FSB / PCIE / VGA / DMI
8	Intel Bearlake - Memory
9	Intel Bearlake - Power
10	Intel Bearlake - GND
11	DDR III DIMM 1 Channel A
12	DDR III DIMM 2 Channel B
13	ICH9 - PCI / DMI / USB / PCIE
14	ICH9 - CPU / SATA / RTC / MSIC
15	ICH7 - POWER / GND
16	PCI - Express X16 Slot / X4 Slot
17	PCI - Express X1 Slot
18	PCI Slot 1 / PCI Slot 2
19	PCI - Express LAN RTL8111B
20	PCI - Express IDE / SATA - 88SE6111
21	PCI IEEE-1394 VT6308
22	Azalia Code ALC888 / ALC88T
23	LPC I/O - F71882FG
24	On Board VGA Connector
25	USB Connector
26	FDD / IDE / SATA / eSATA / FANConnector
27	VRM 11 - ISL6322CR
28	ACPI Controller UPI
29	UPI Switch Power
30	ATX POWER / Panel / SMBUS ISO

2007.04.16

MODEL Config.	ORCAD Config.	Function	Option	ERP Number	PCB	
MS7356 STD	cfg7356-std	Intel G33(A1) + ICH9R(A1) + IEEE1394 + ALC888	STD	601-7356-B10.001	Red v0B	CH
MS7356 A	cfg7356-a	Intel P35(A1) + ICH9R(A1) + IEEE1394 + ALC888T	A	601-7356-B20.001	Red v0B	CH

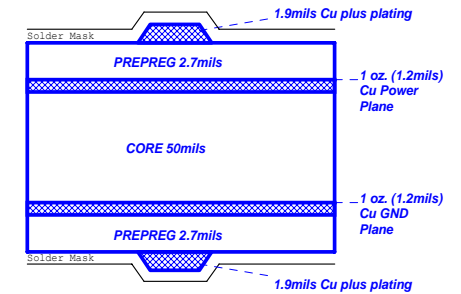
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Title			
<b>Cover Sheet</b>			
Size	Document Number		Rev
Custom	<b>MS-7356</b>		<b>10</b>
Date:	Monday, April 16, 2007	Sheet	1 of 36

# Block Diagram

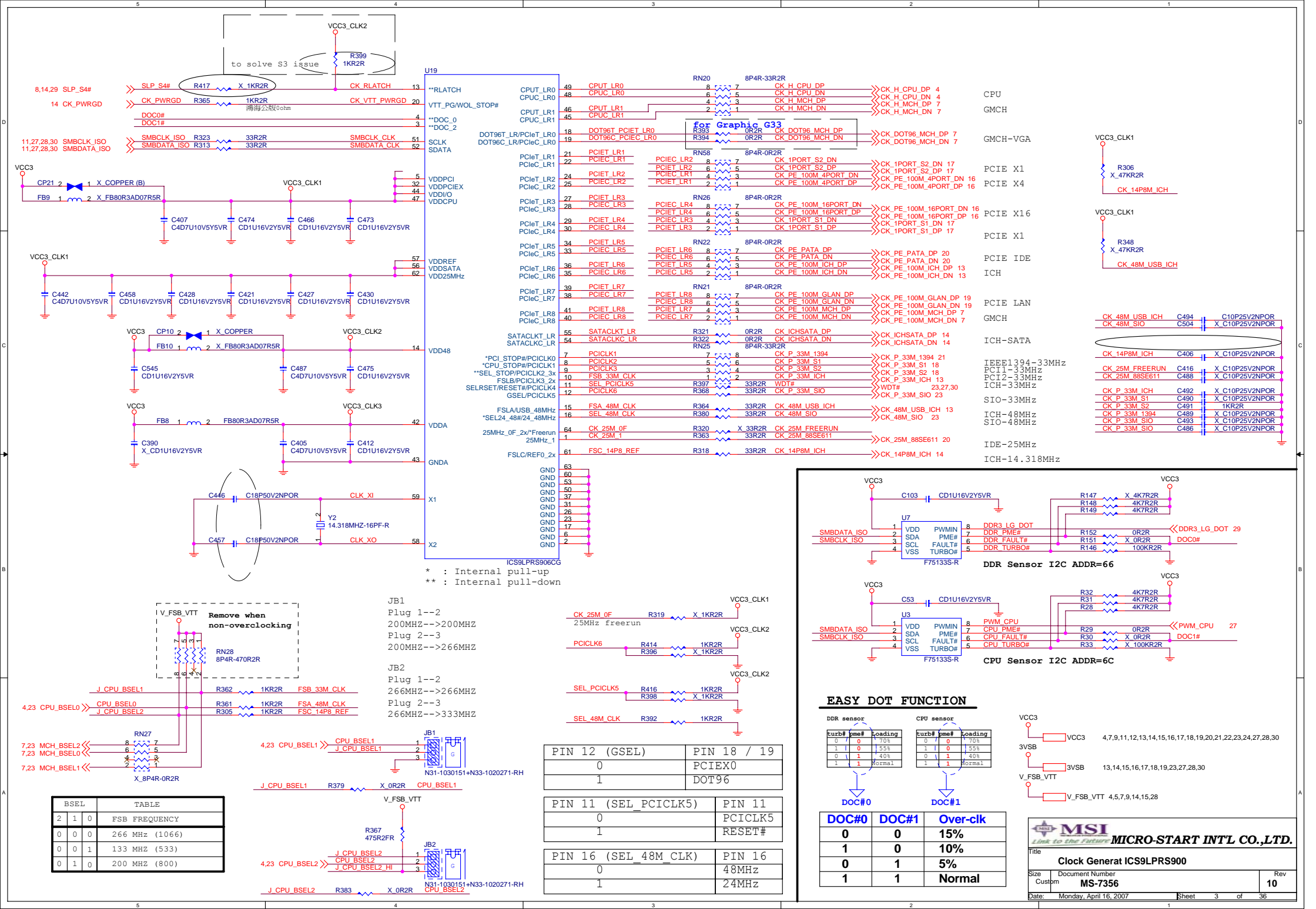


## Board Stack-up

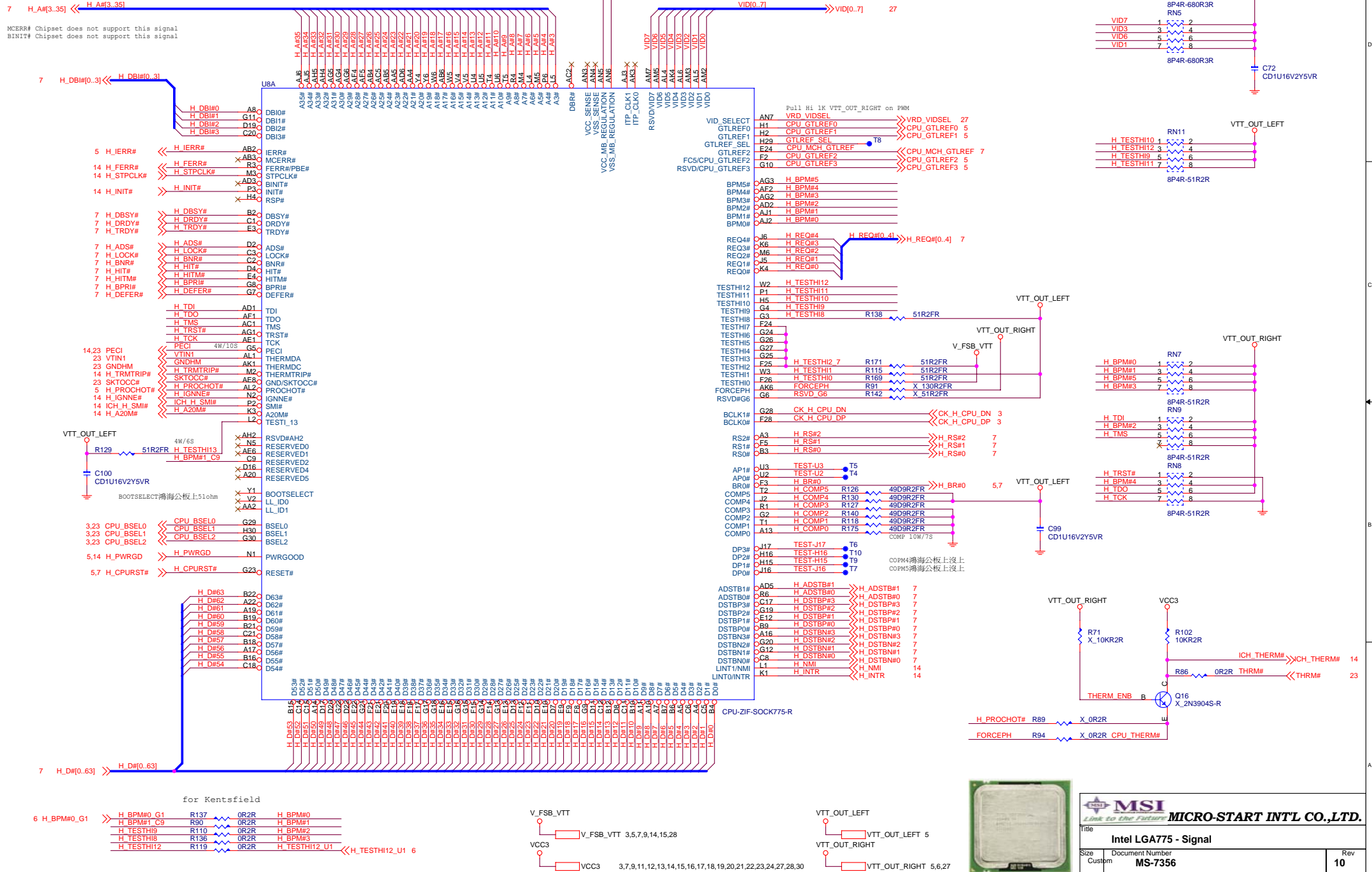
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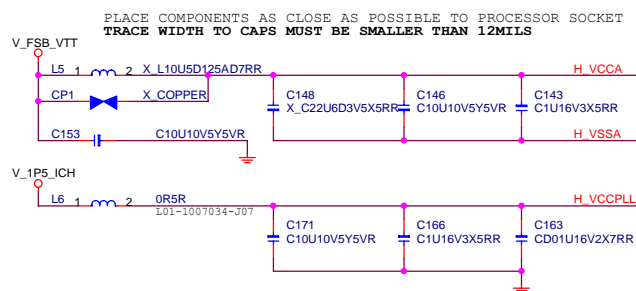
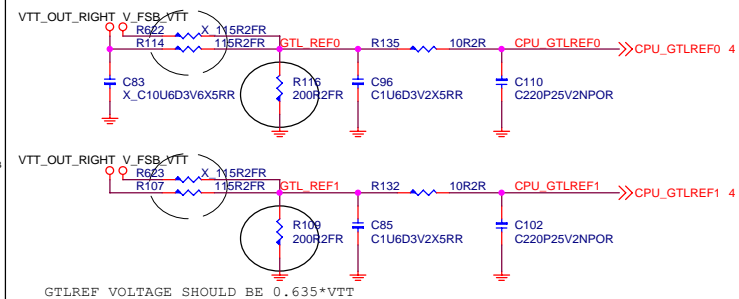


Single End 50ohm Top/Bottom : 4mils  
 USB2.0 - 90ohm : 15/4.5/7.5/4.5/15  
 SATA - 95ohm : 15/4/8/4/15  
 LAN - 100ohm : 15/4/8/4/15  
 PCIE - 95ohm : 15/4/8/4/15  
 IEEE1394 - 110ohm : 15/4/9/4/15  
 IDE : 15/4/8/4/15

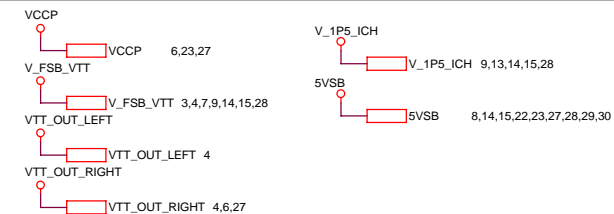
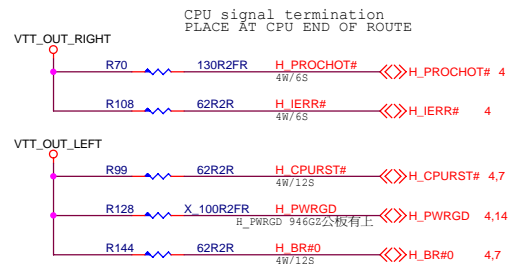
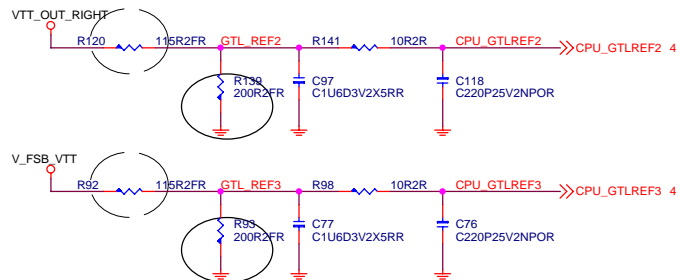
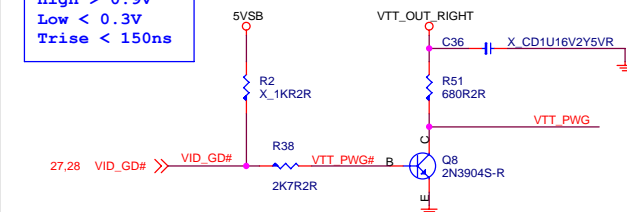



### CPU SIGNAL BLOCK





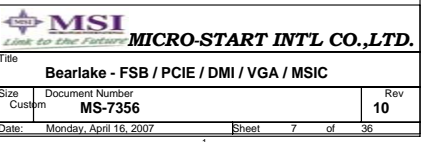
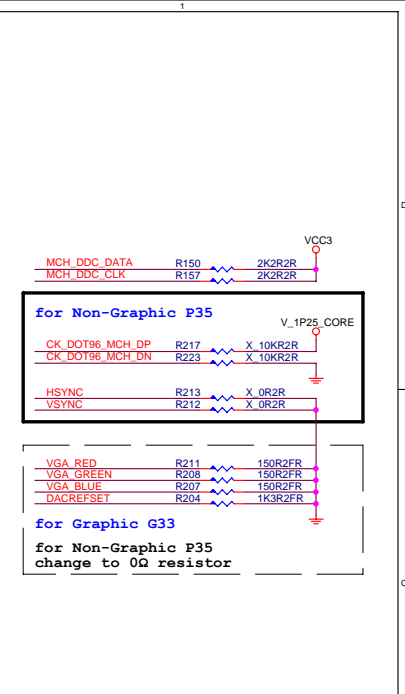
```
VTT_PWG SPEC :
High > 0.9V
Low < 0.3V
Trise < 150ns
```



 <b>MSI</b> Link to the Future				<b>MICRO-START INT'L CO.,LTD.</b>			
Title							
Intel LGA775 - Power							
Size		Document Number				Rev	
Custom		MS-7356				10	
Date: Monday, April 16, 2007				Sheet 5 of 36			

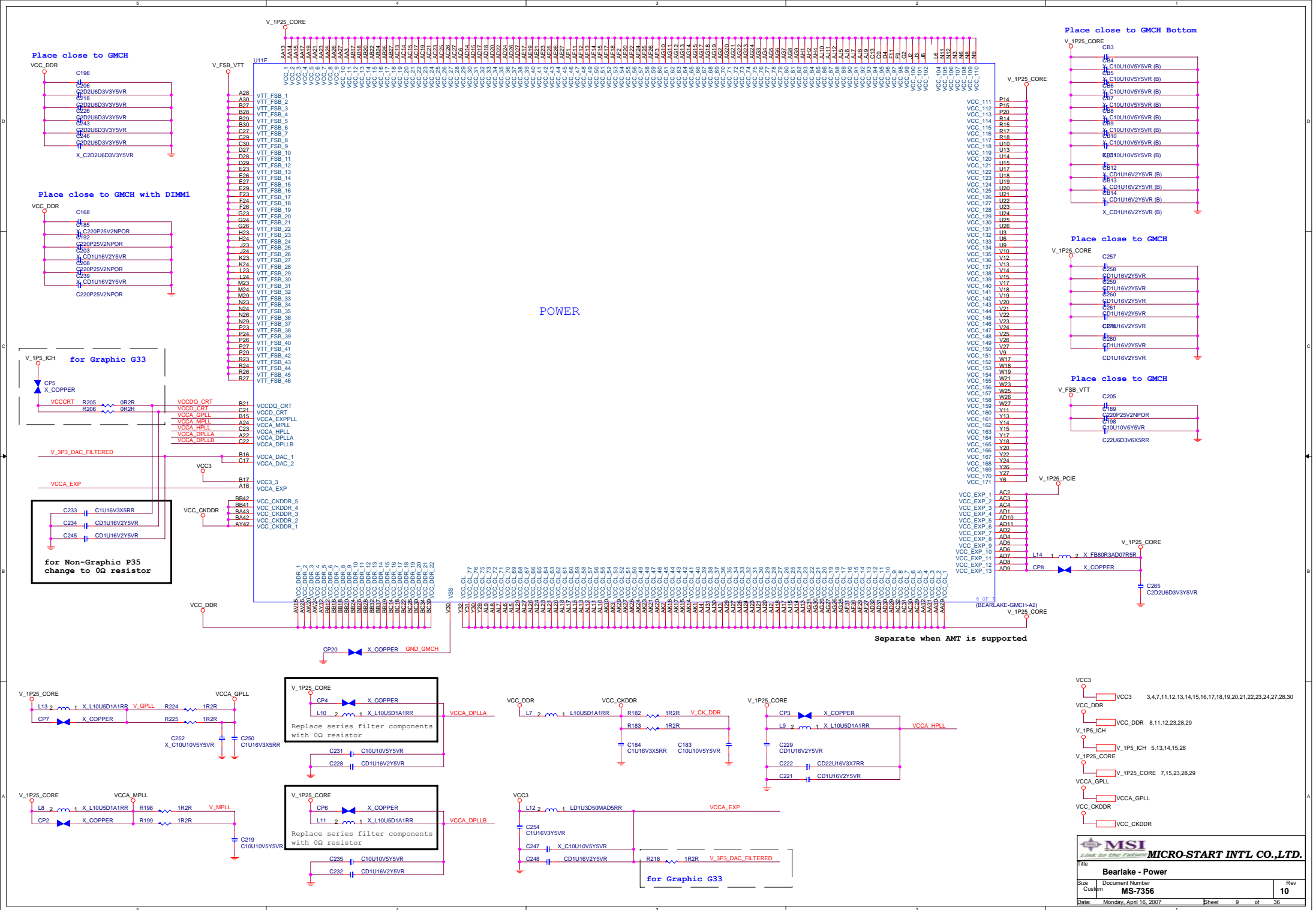


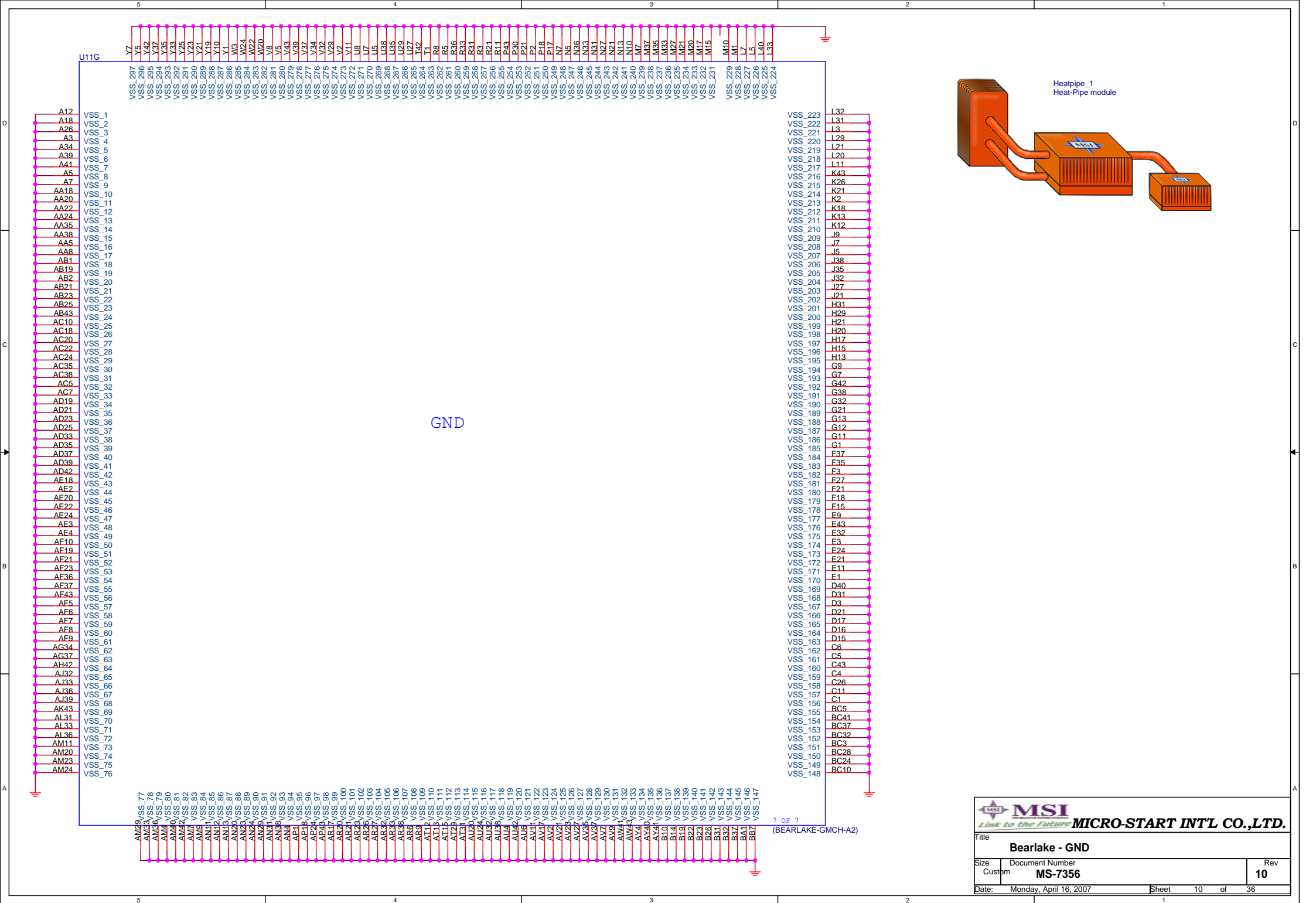







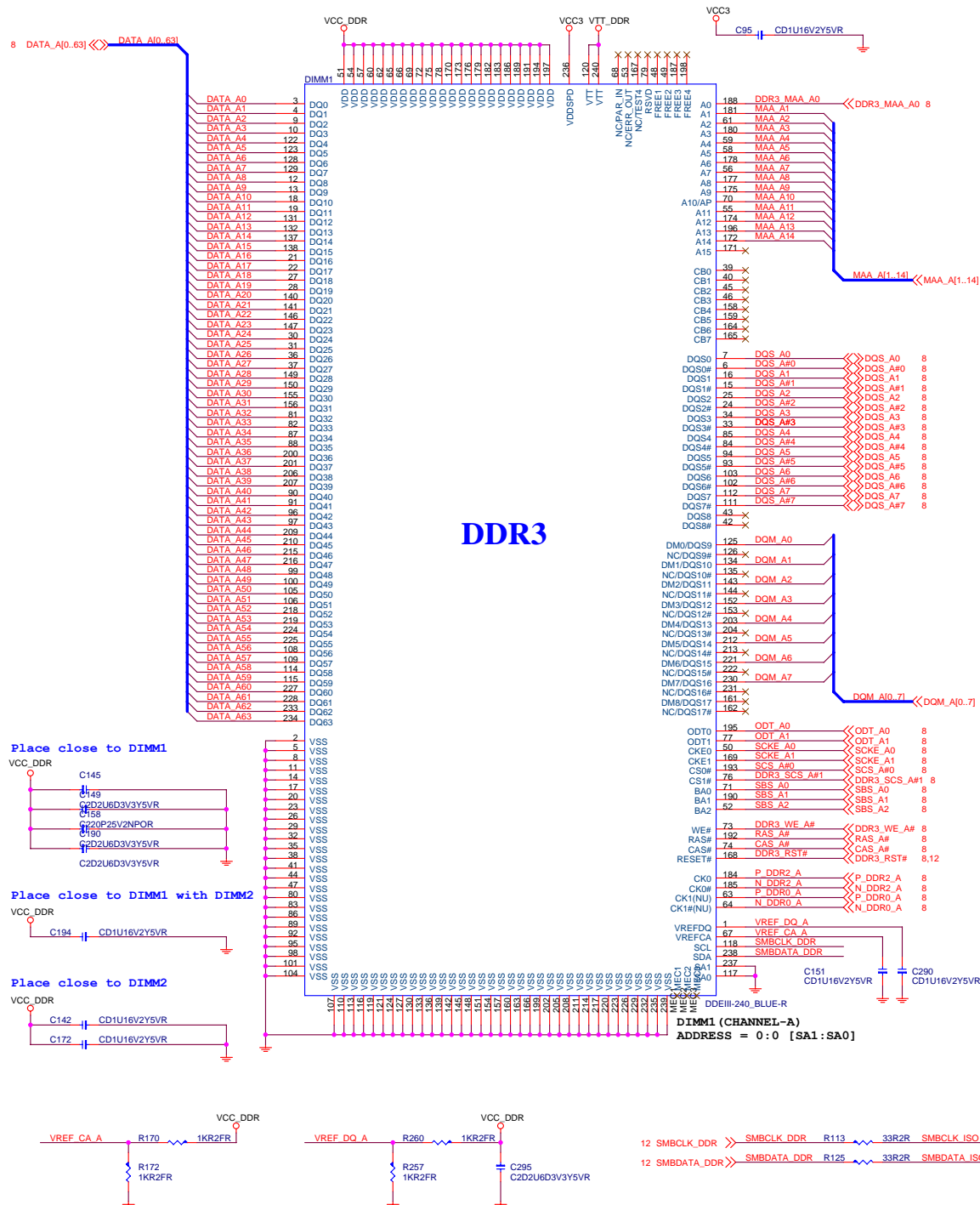




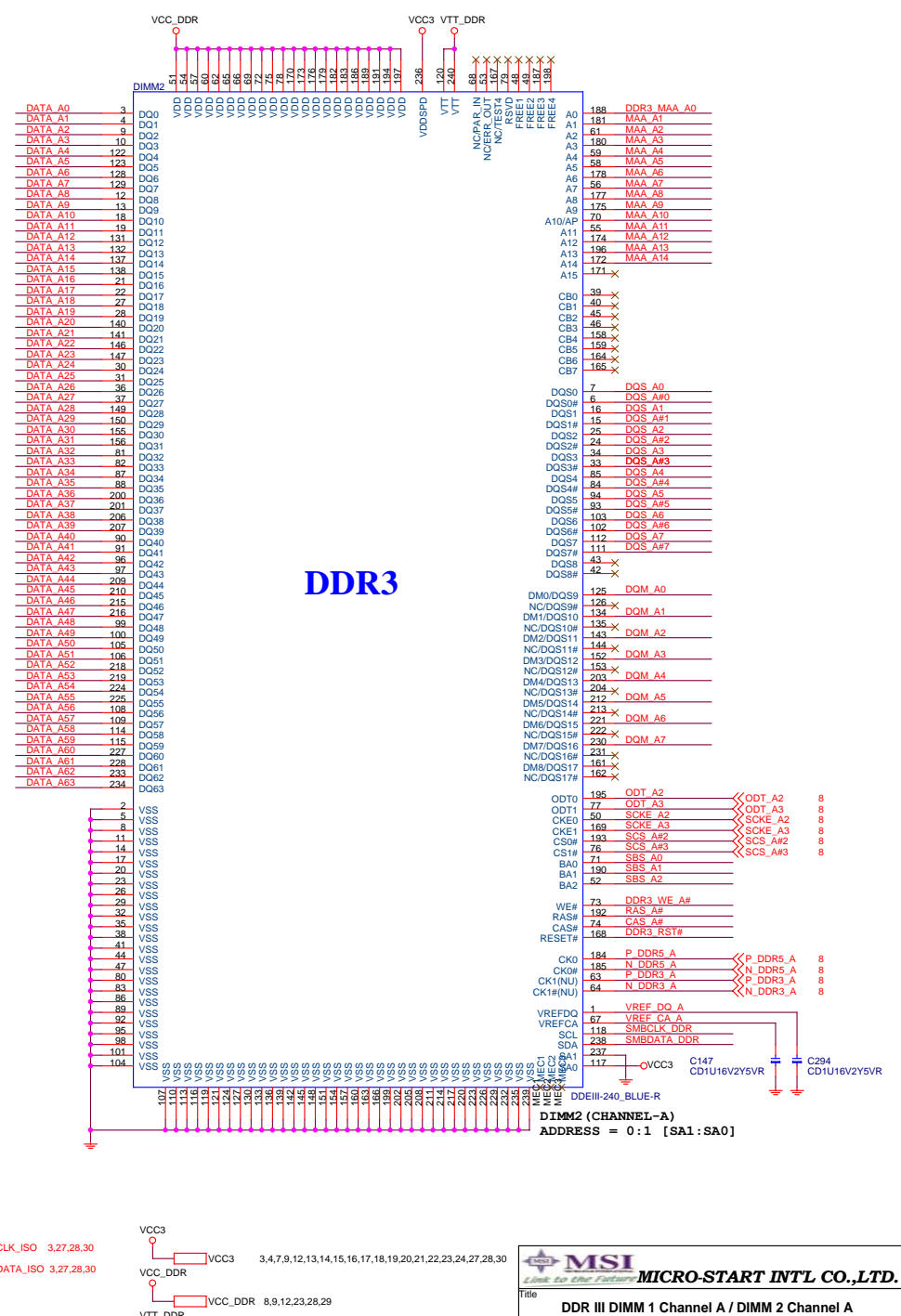


 <b>MICRO-START INTL CO.,LTD.</b>		
Title		
Bearlake - GND		
Size	Document Number	Rev
Custom	MS-7356	10
Date:	Monday, April 16, 2007	Sheet 10 of 36

## DDRIII DIMM\_A1

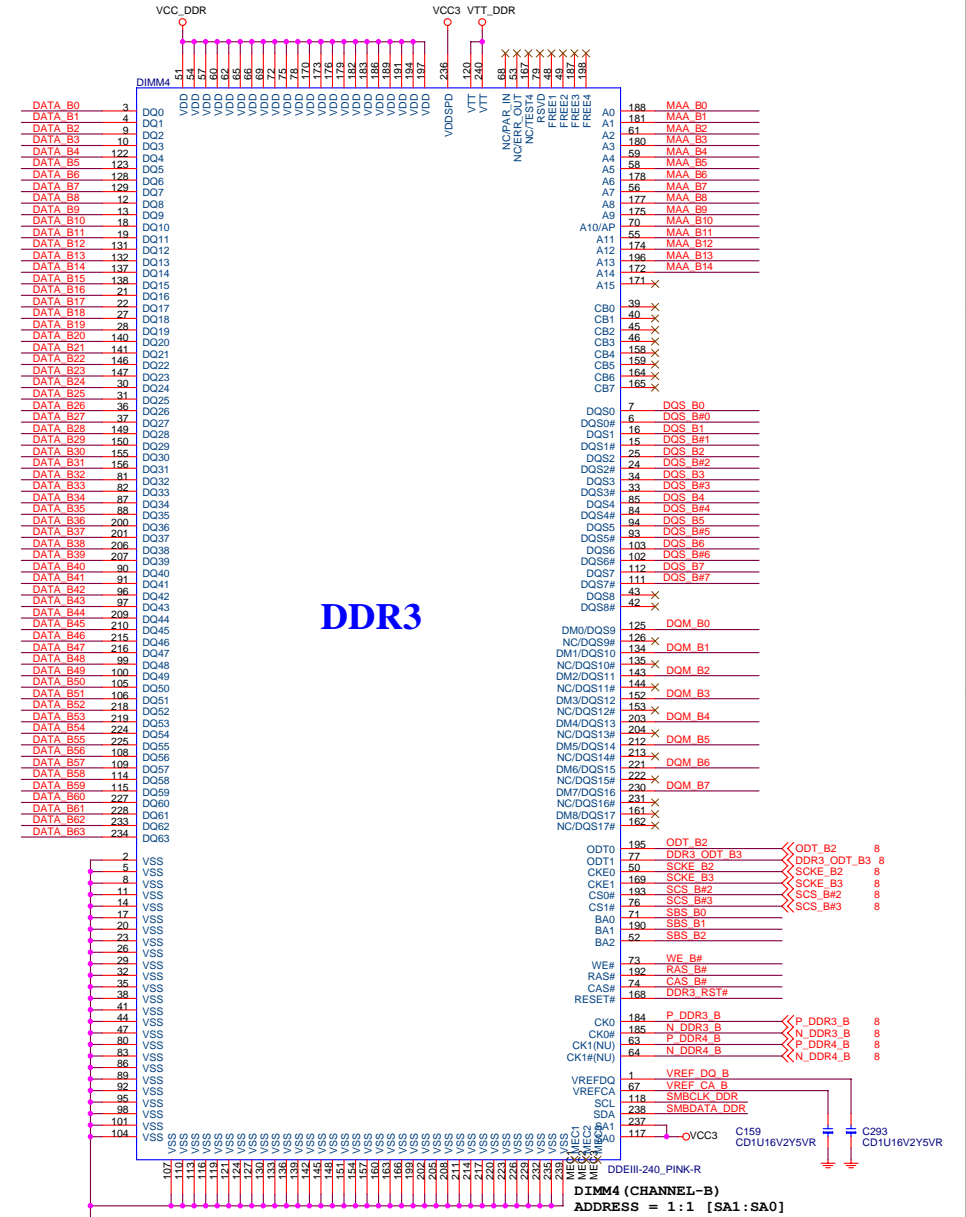
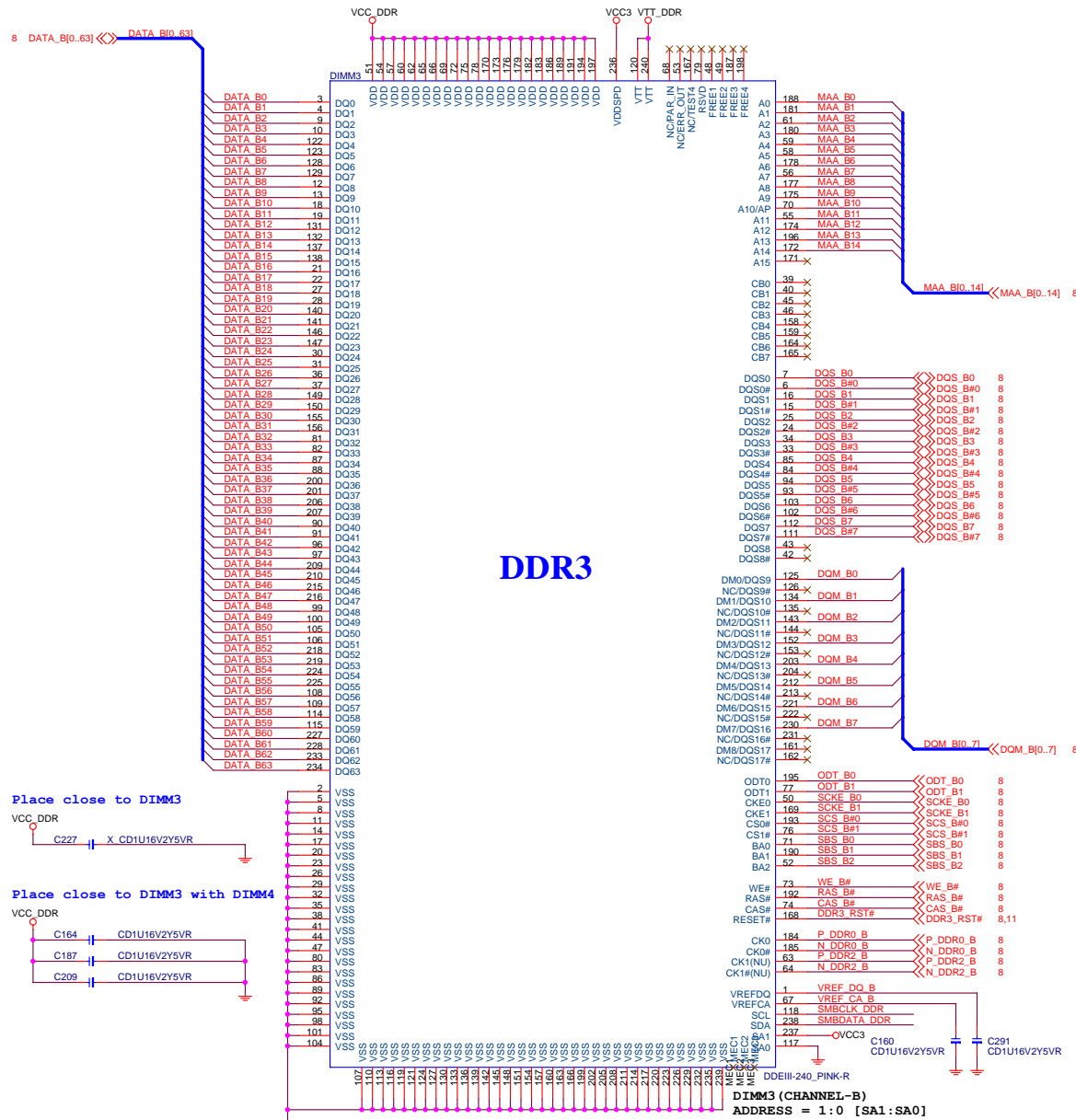


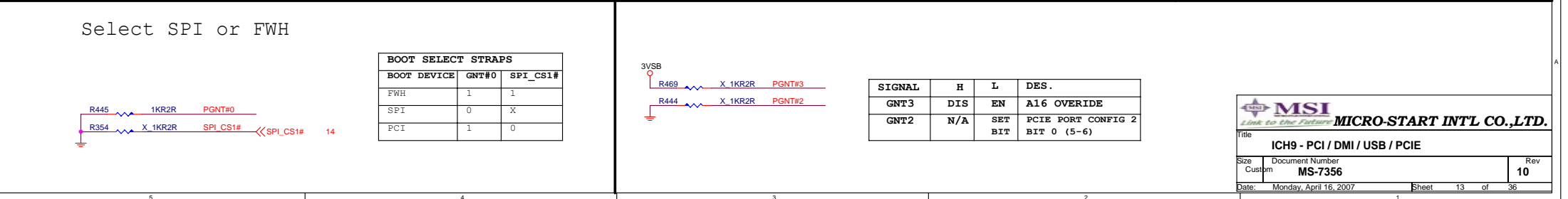
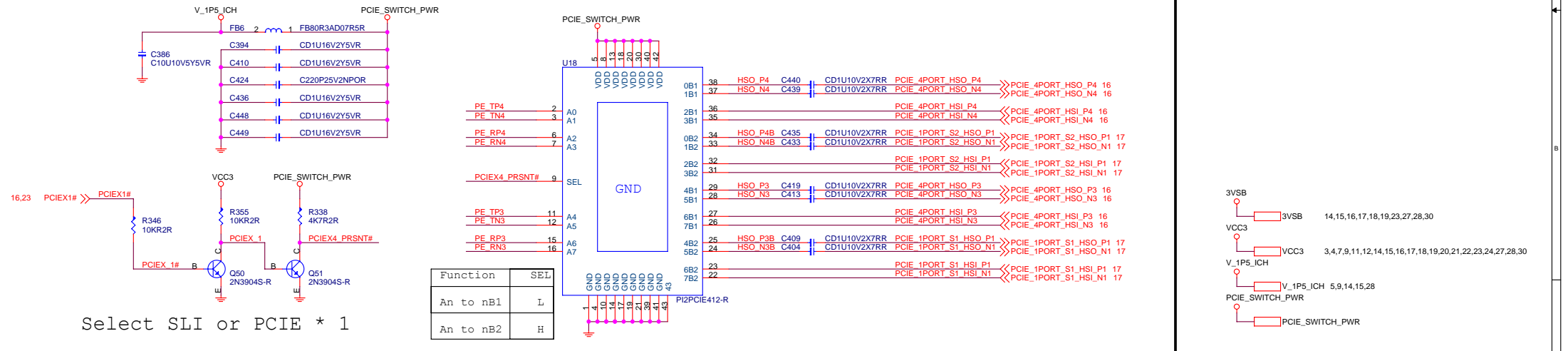
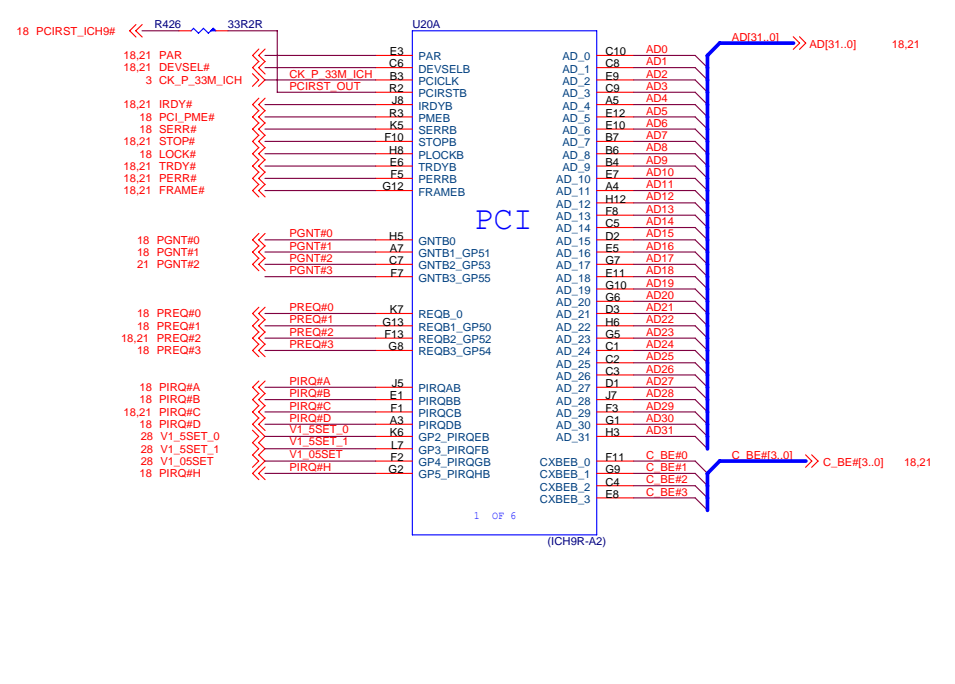
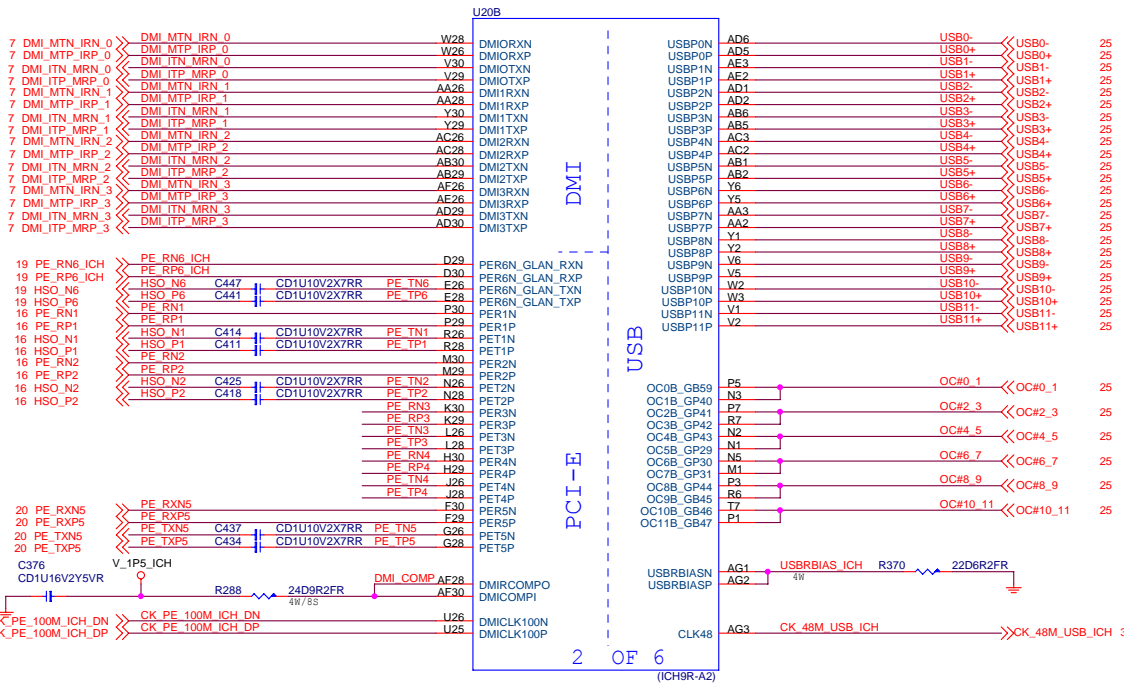
## DDRIII DIMM\_A2



# DDR3 DIMM\_B1

# DDR3 DIMM\_B2





BOOT SELECT STRAPS		
BOOT DEVICE	GNT#0	SPI_CS1#
FWH	1	1
SPI	0	X
PCI	1	0

SIGNAL	H	L	DES.
GNT3	DIS	EN	A16 OVERRIDE
GNT2	N/A	SET BIT	PCIE PORT CONFIG 2 BIT 0 (5-6)

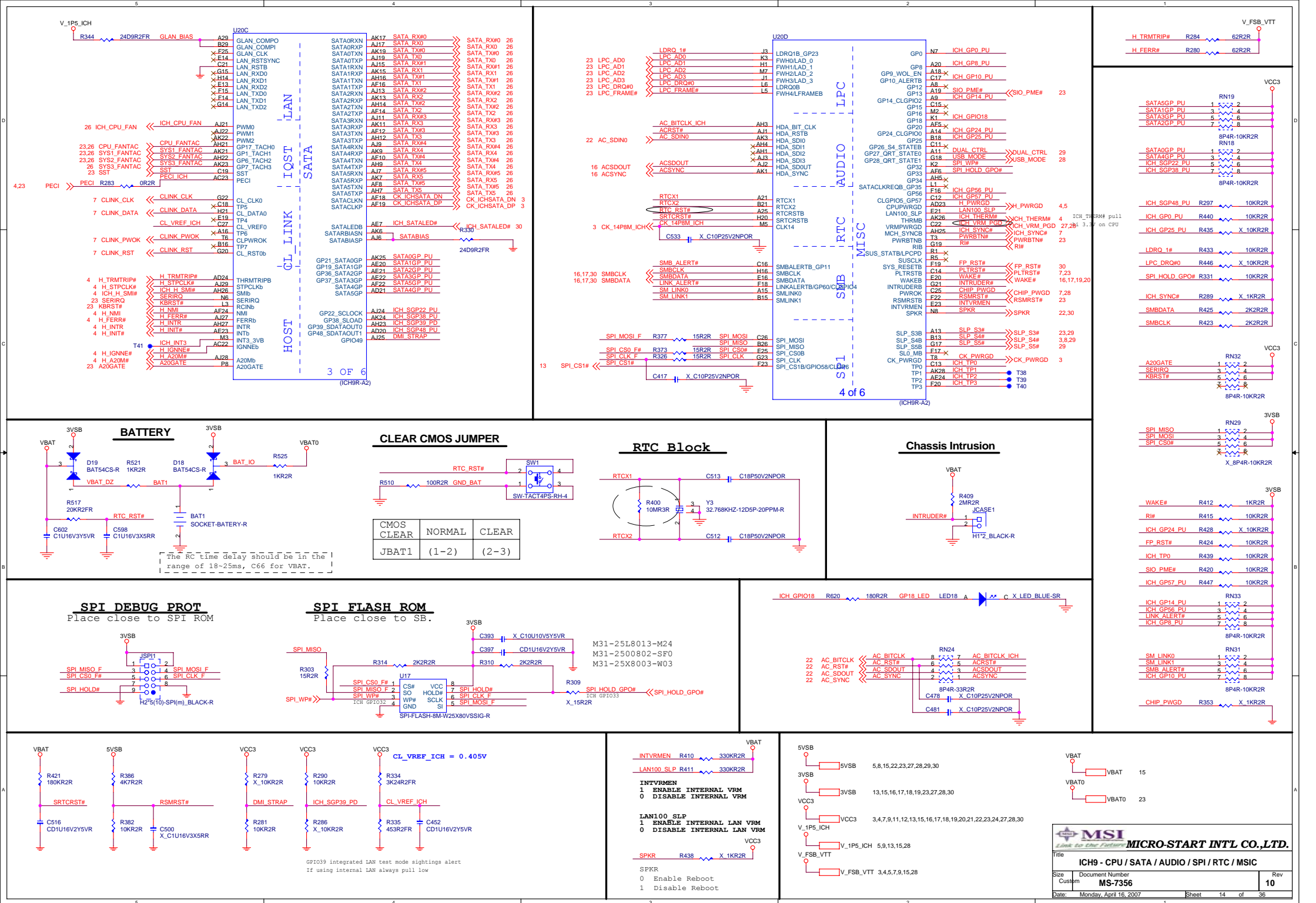
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Link to the Future  
**MICRO-START INTL CO.,LTD.**

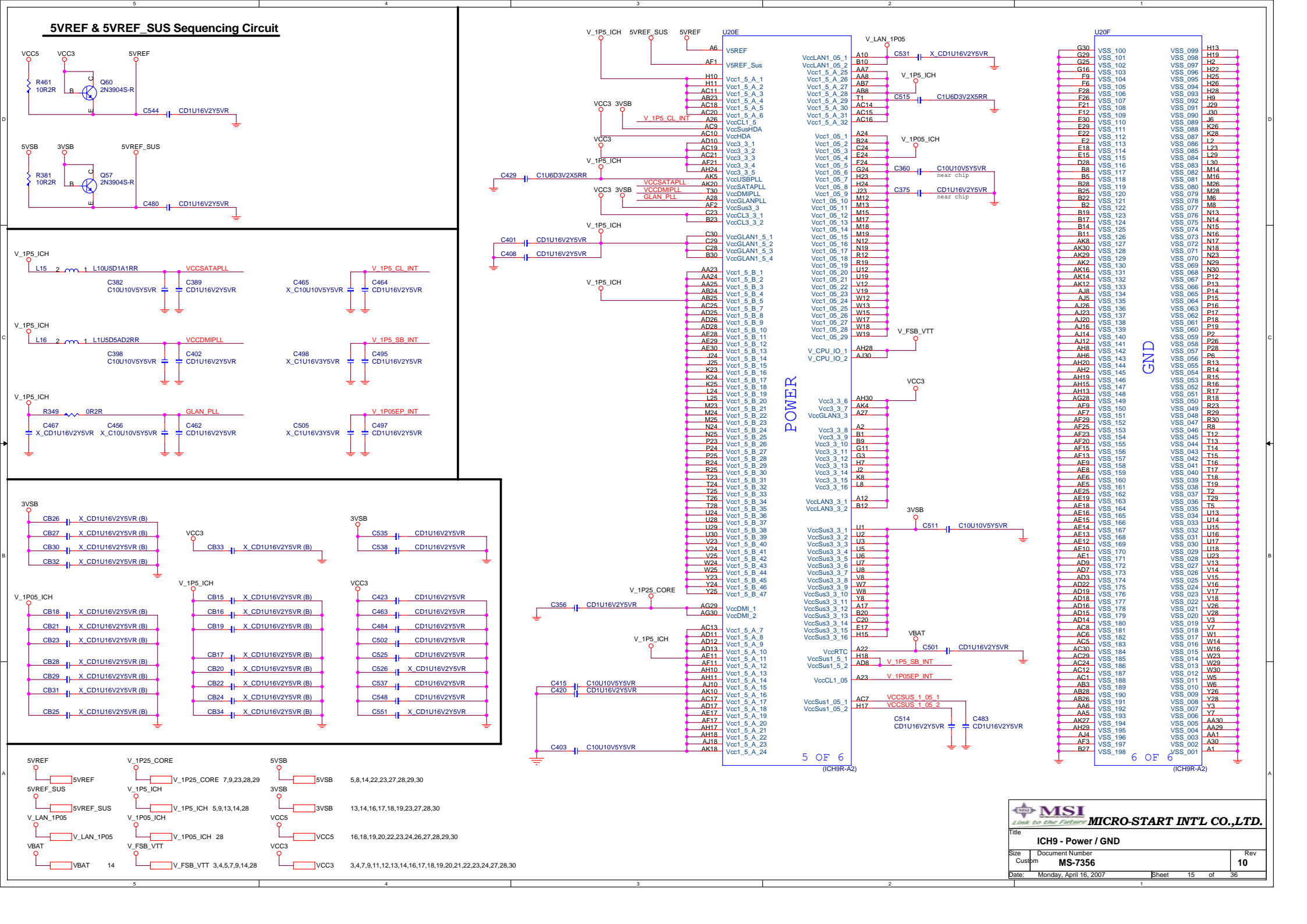
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Size: Document Number **MS-7356** Rev **10**

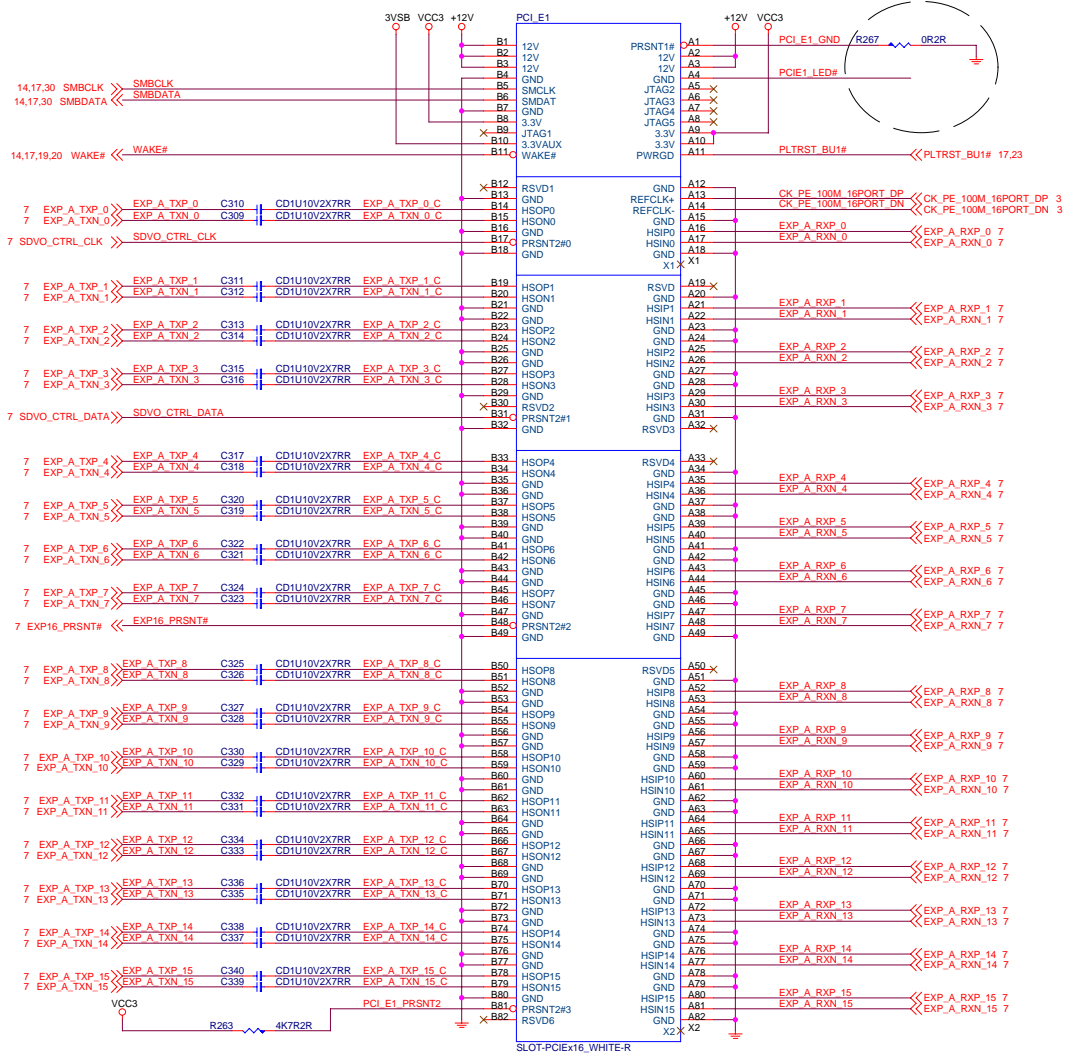
Date: Monday, April 16, 2007 Sheet 13 of 36





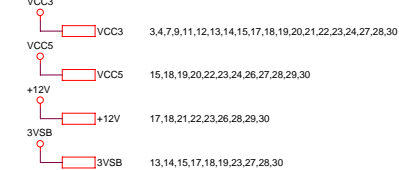
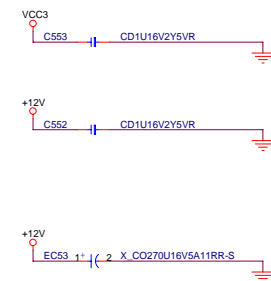
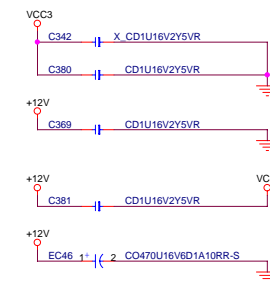
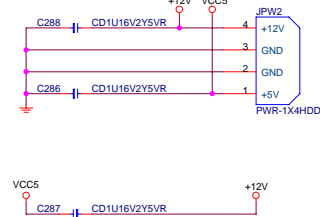
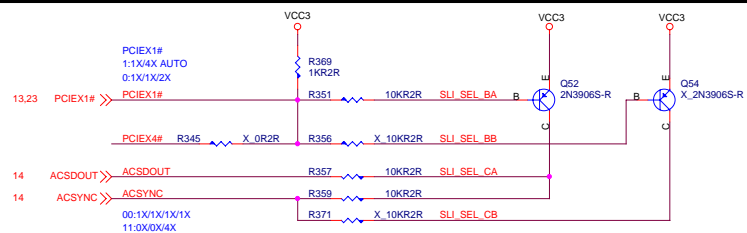
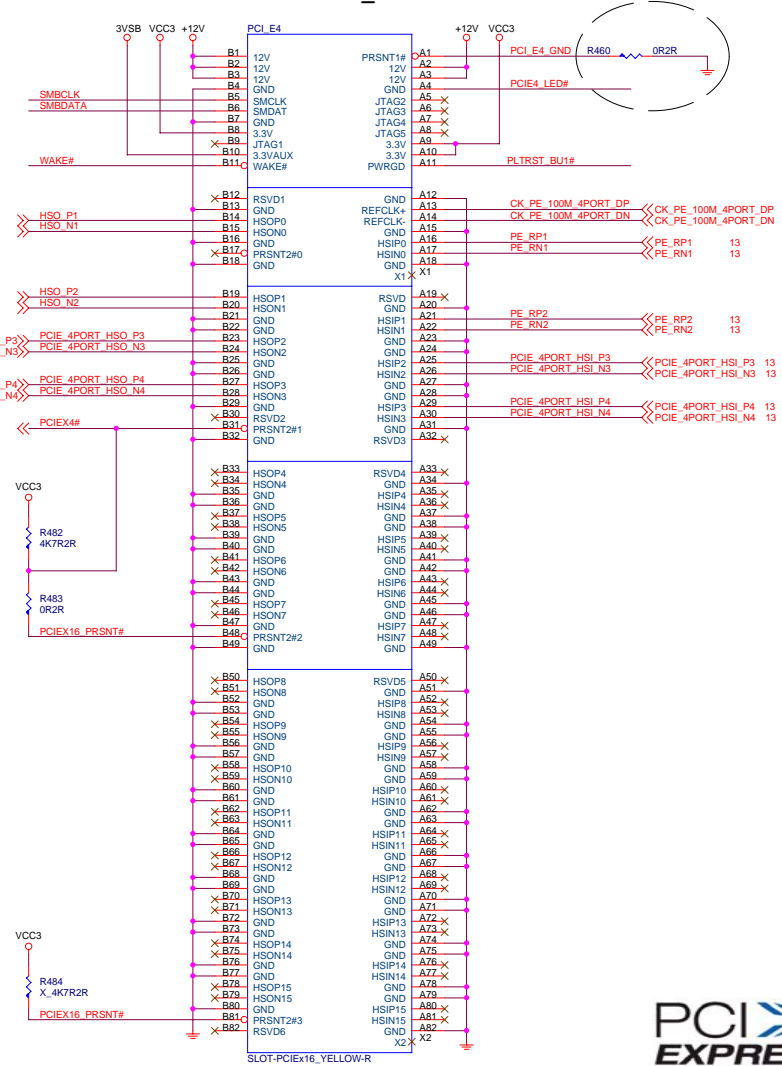
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PCI Express X16 Slot

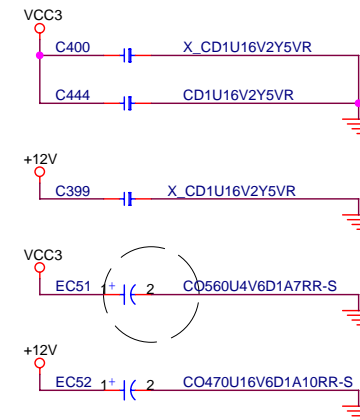
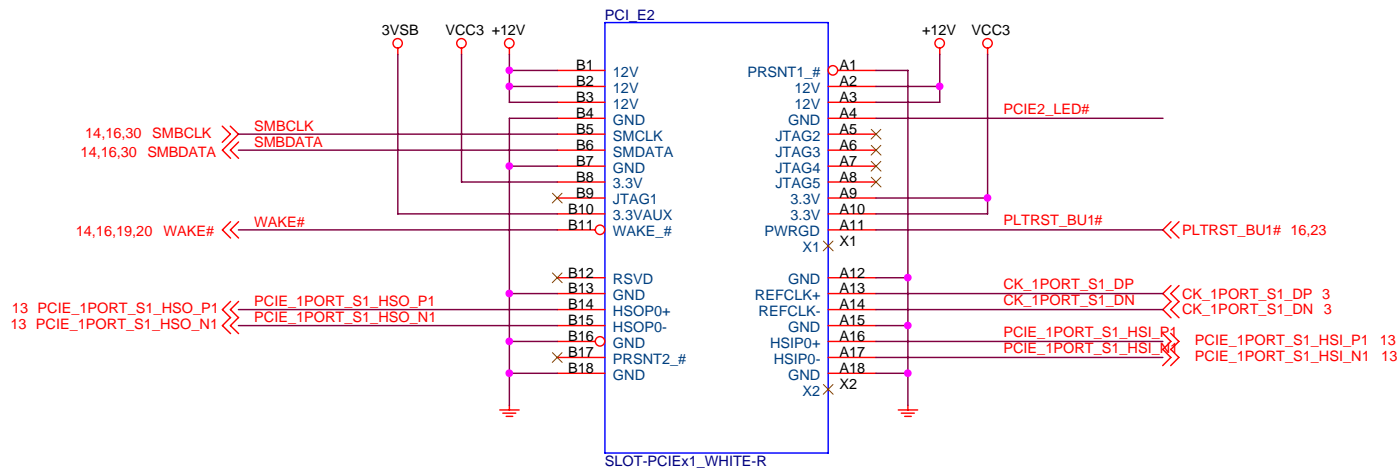


PCI Express X4 Slot

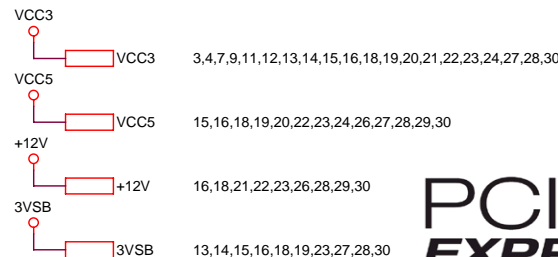
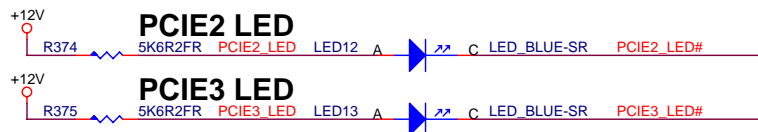
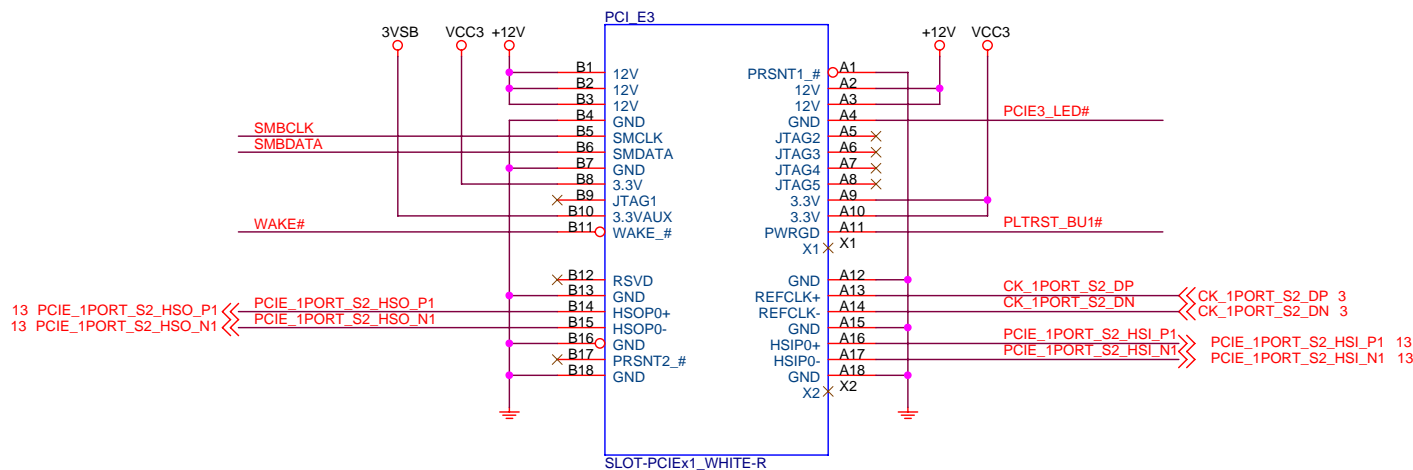
(Share with PCI\_E x1 Slots)





## PCI EXPRESS x1-PORT

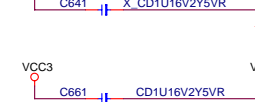
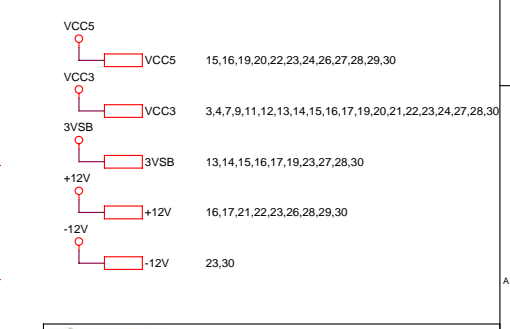
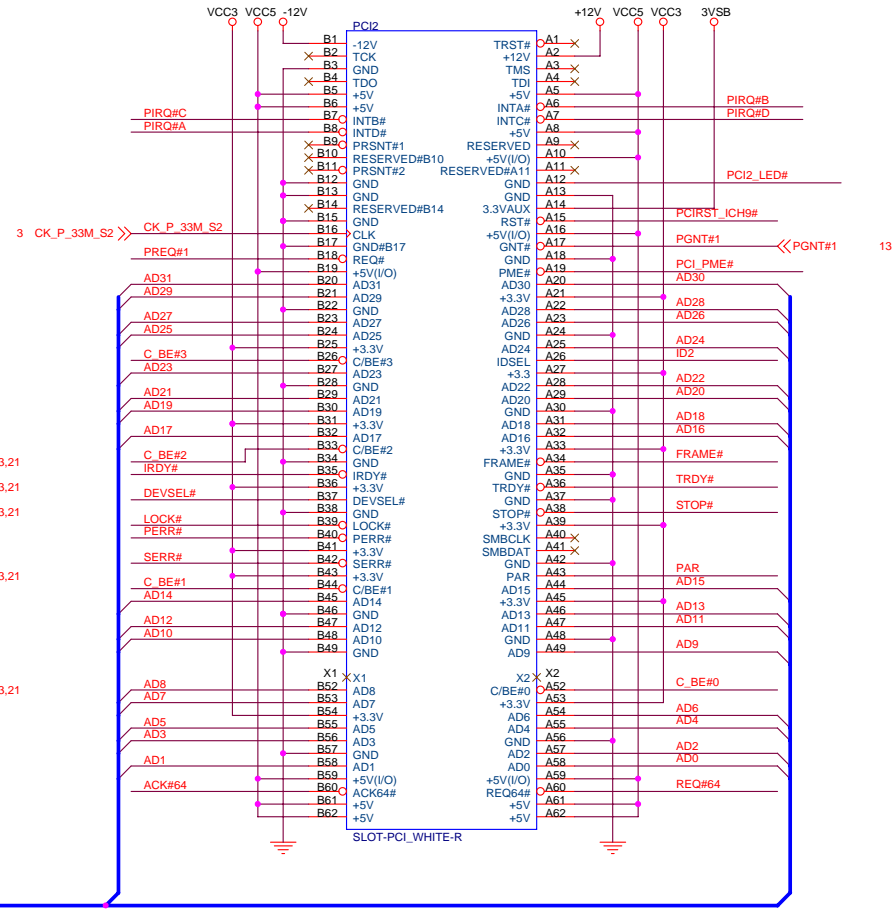


## PCI EXPRESS x1-PORT

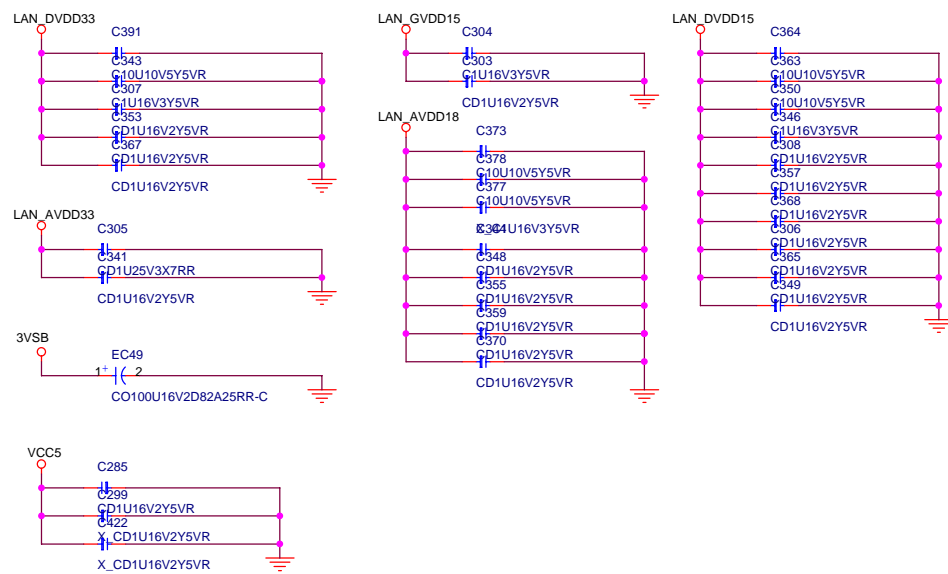


 		<b>MICRO-STAR INT'L CO.,LTD.</b>	
<i>Link to the Future</i>			
Title			
<b>PCI EXPRESS X1 SLOT</b>			
Size	Document Number	Rev	
Custom	<b>MS-7356</b>	<b>10</b>	
Date:	Monday, April 16, 2007	Sheet	17 of 36

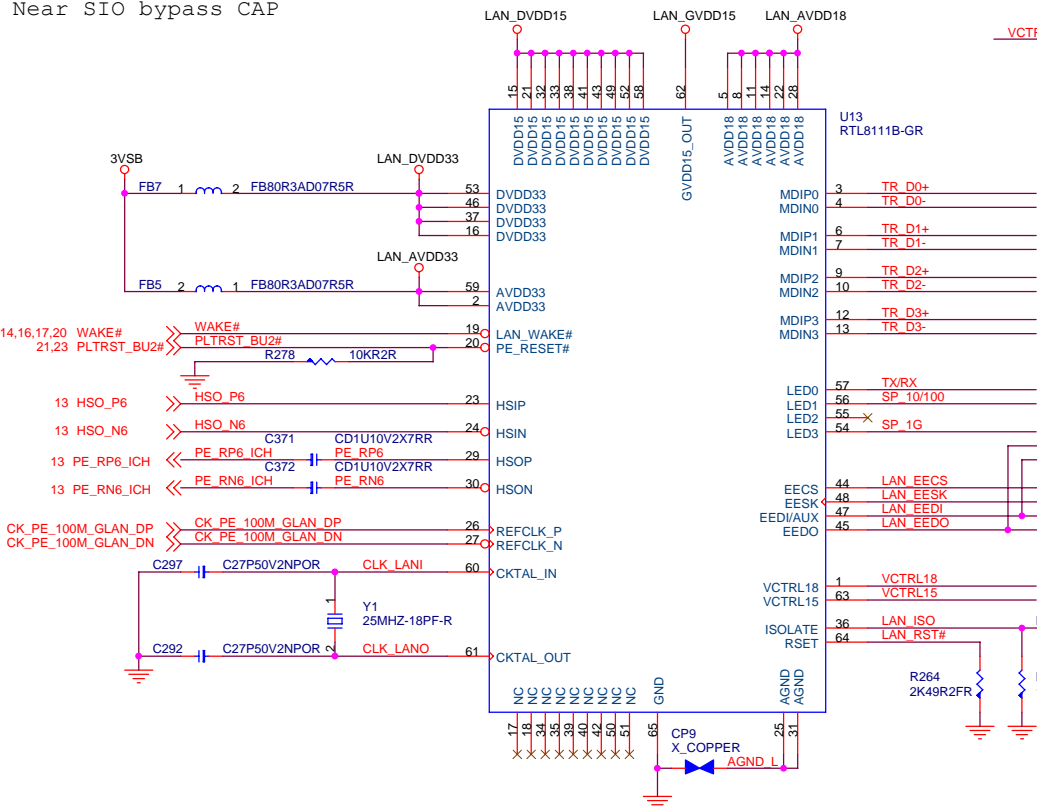
## PCI2



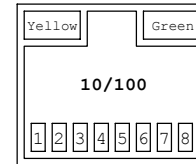
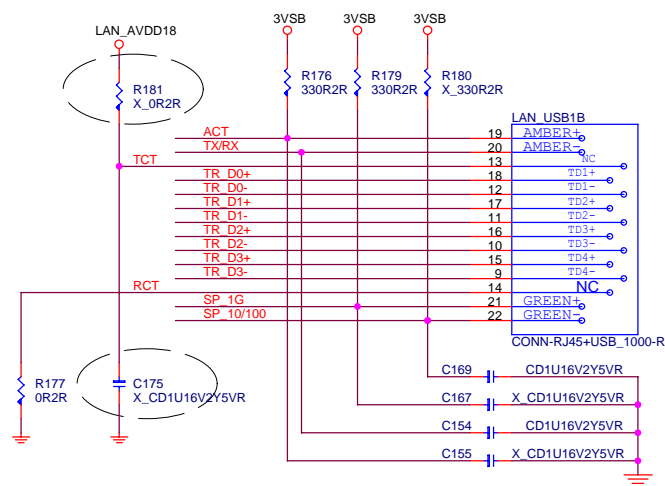




Near SIO bypass CAP

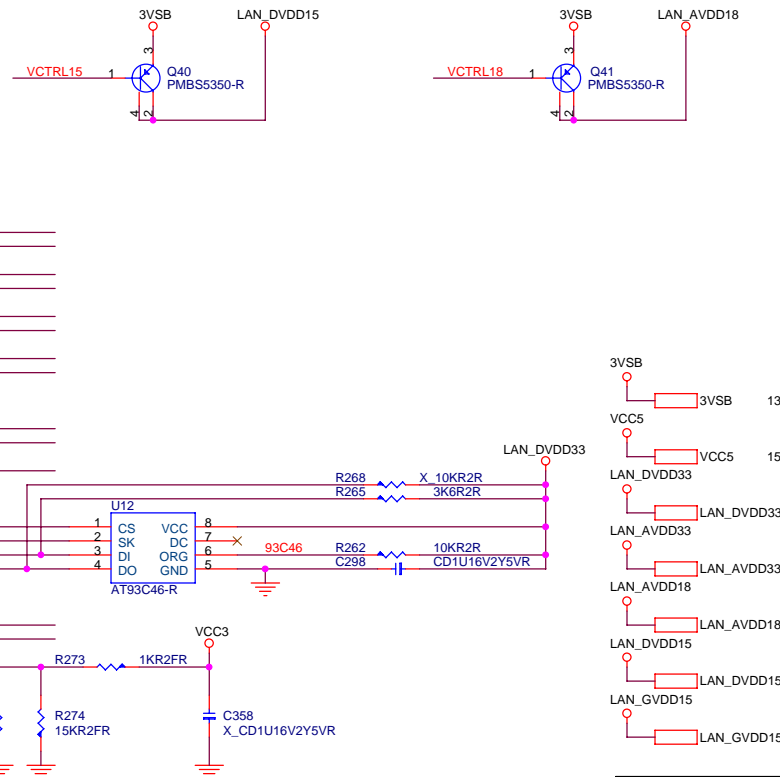


When the ORG pin is connected to VCC, the x 16 organization is selected. When it is connected to ground, the x 8 organization is selected. If the ORG pin is left unconnected and the application does not load the input beyond the capability of the internal 1 Meg ohm pullup, then the x 16 organization is selected. The feature is not available on the 1.8V devices.



for RTL8111B

10/100 : N58-22F0201-S42 RoHS  
1000 : N58-22F0211-S42 RoHS



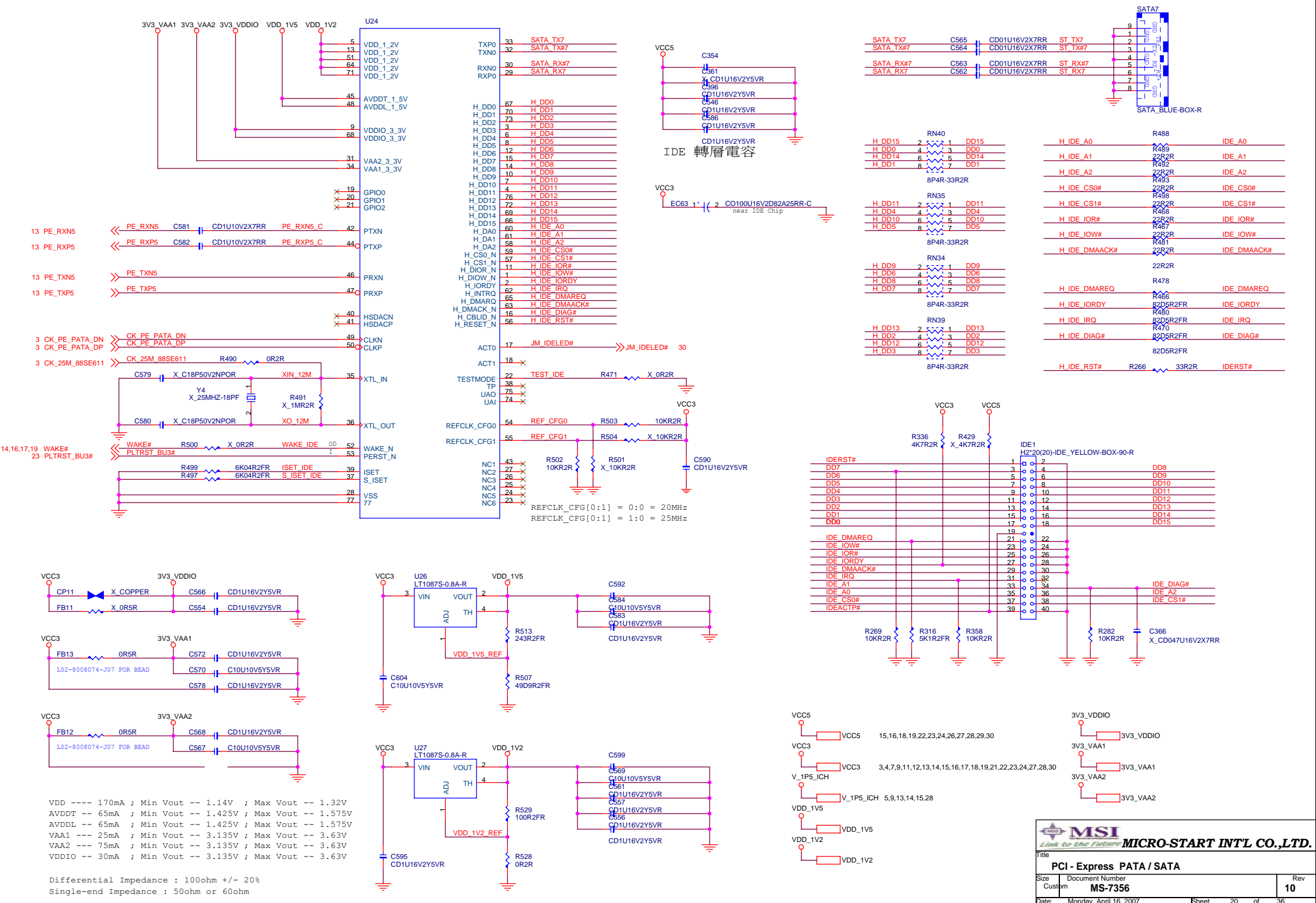
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Link to the Future

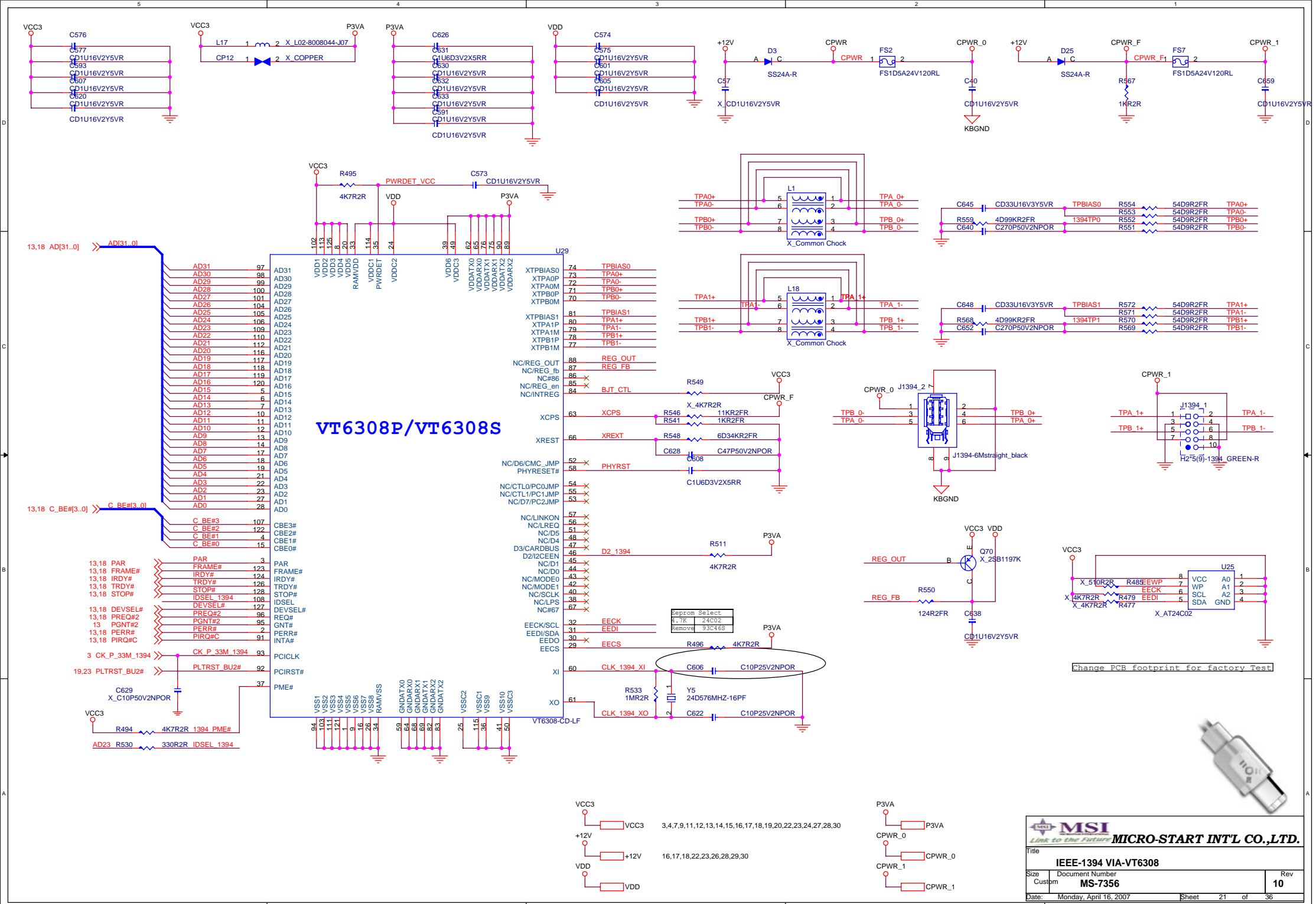
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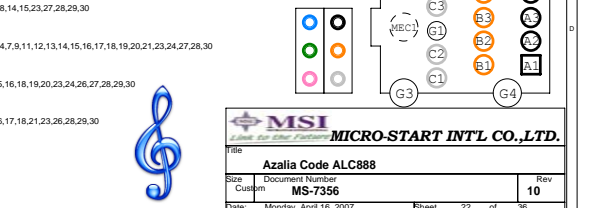
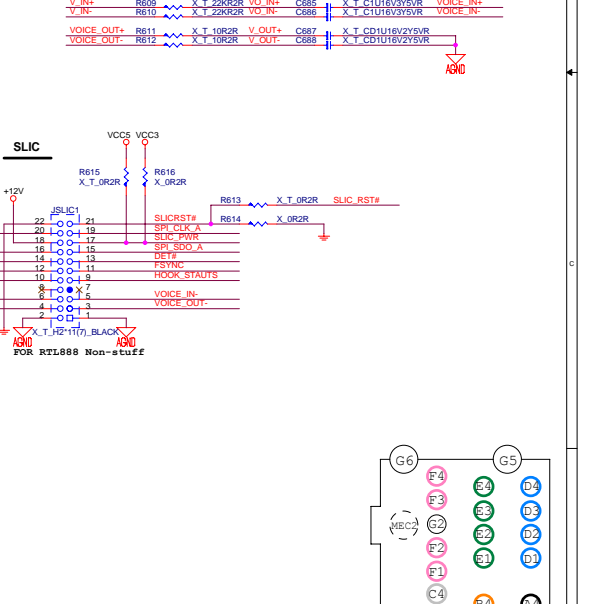
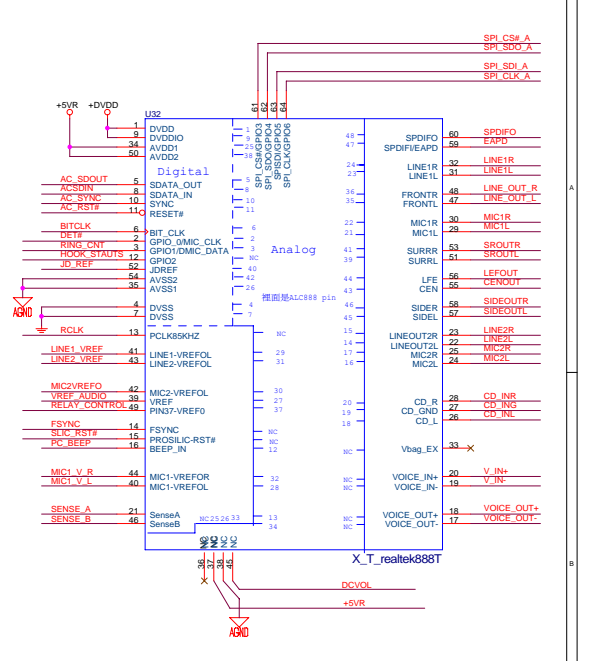
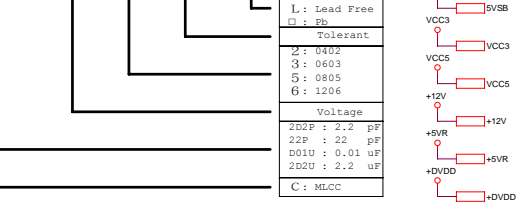
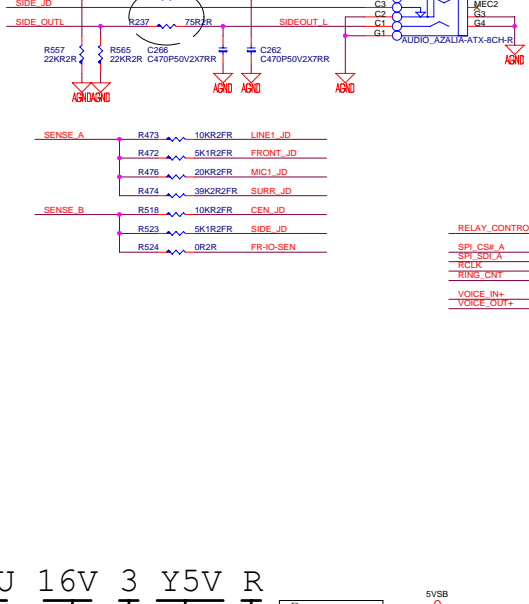
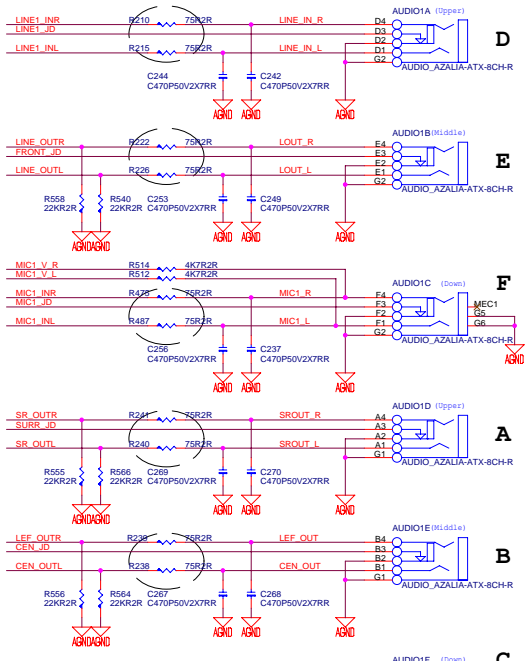
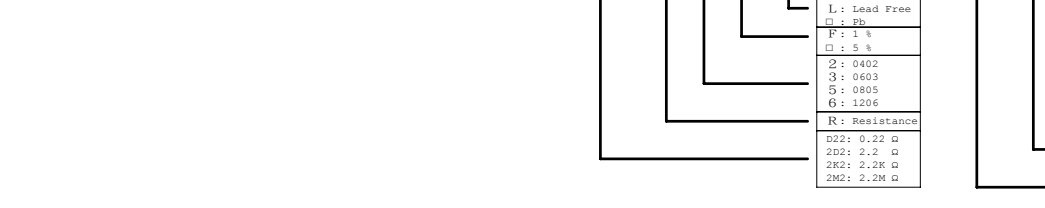
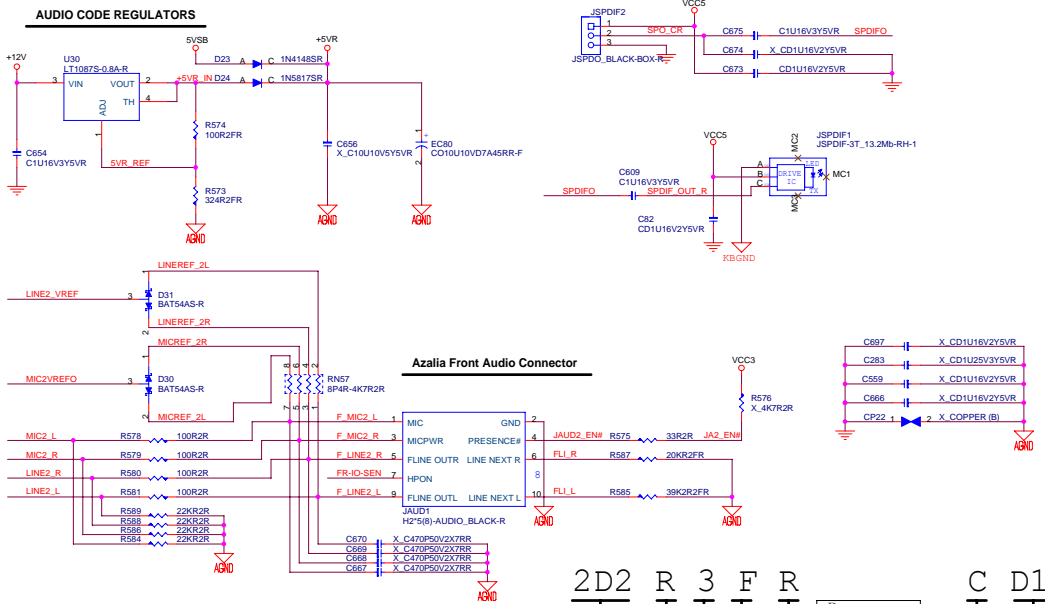
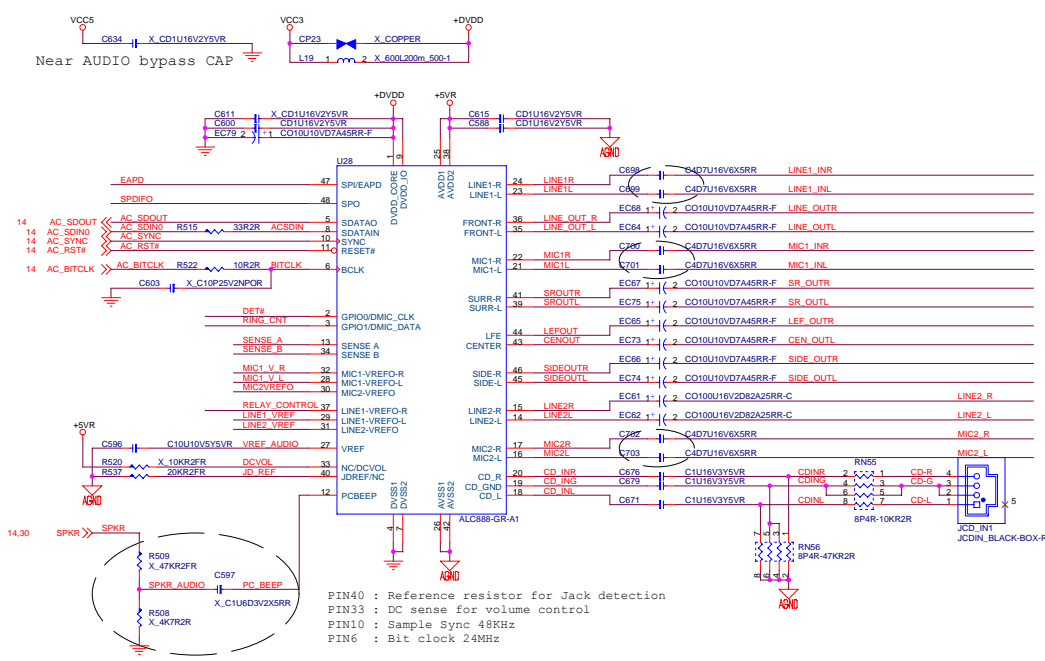
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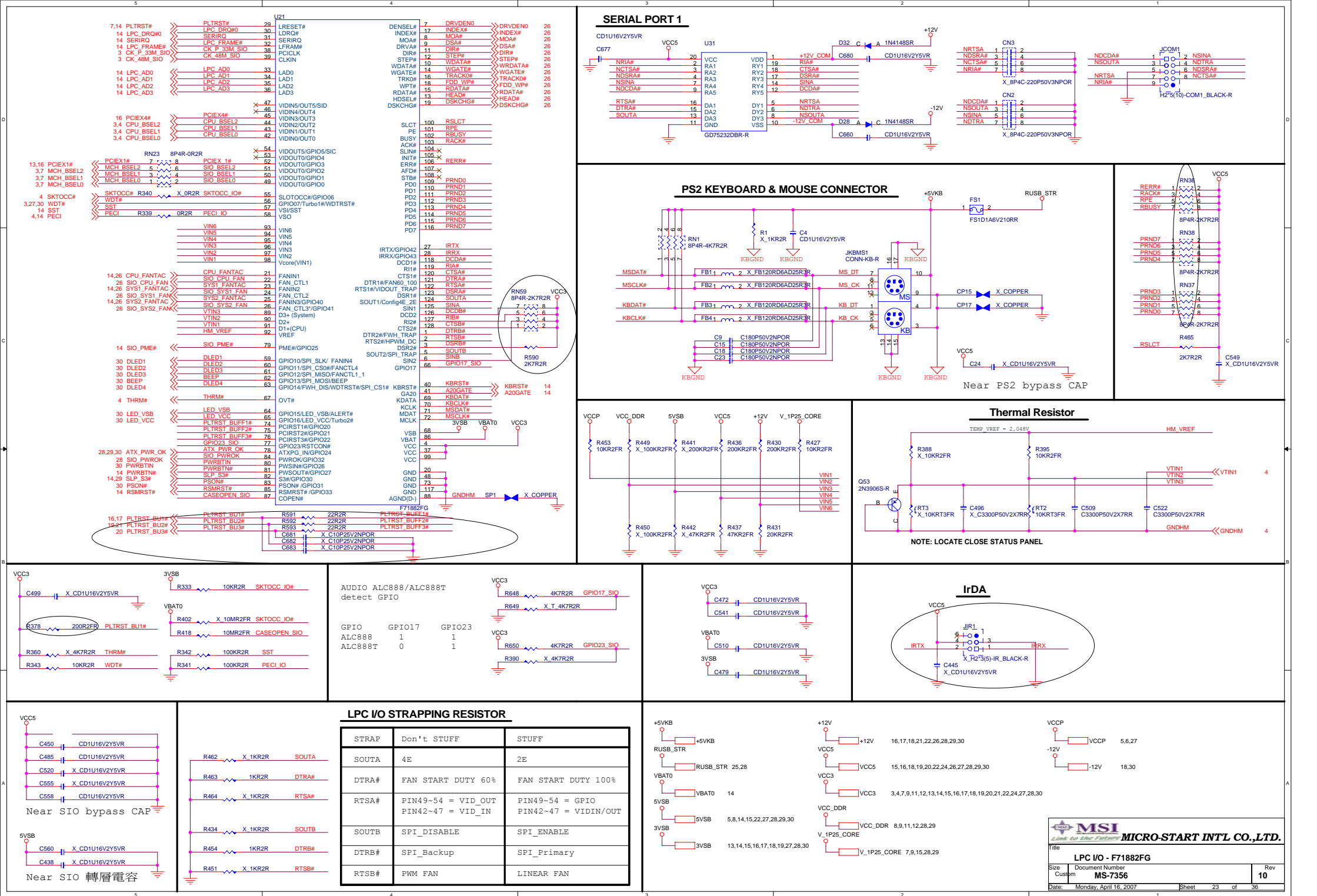
Size: Custom Document Number: **MS-7356** Rev: **10**

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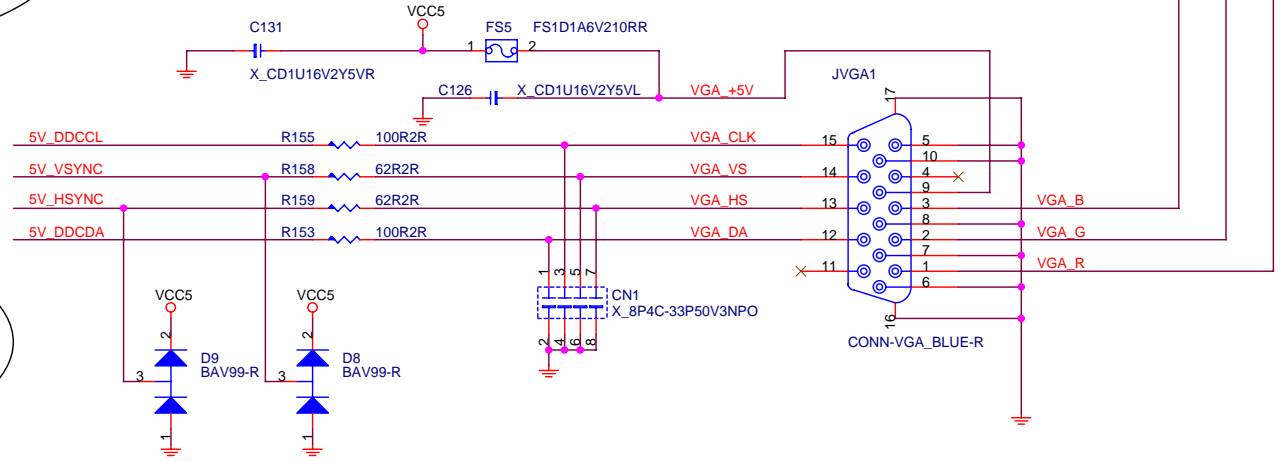
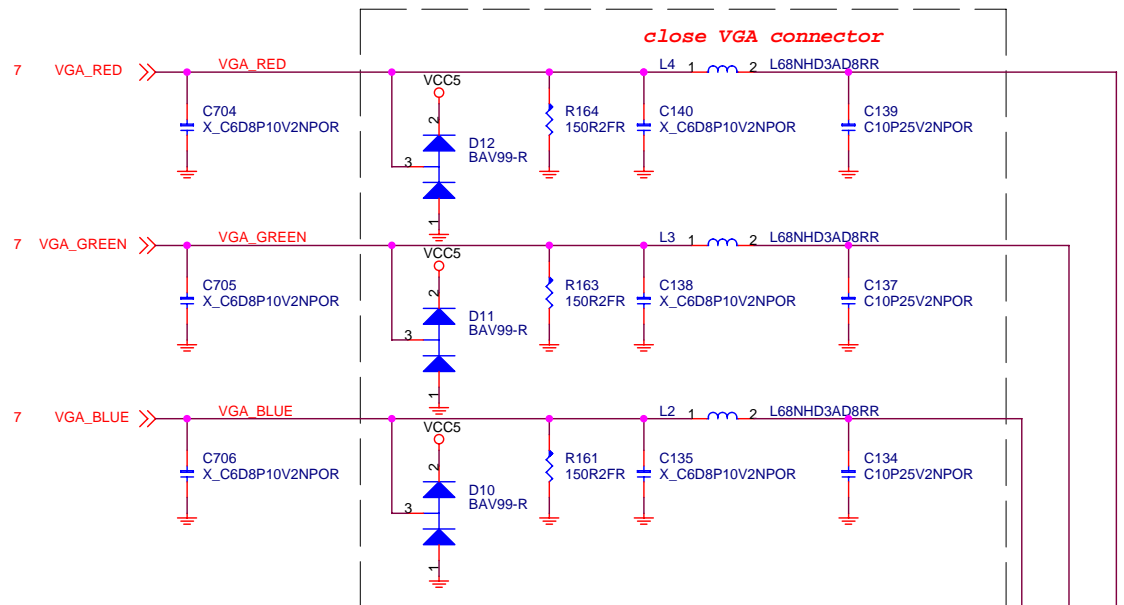
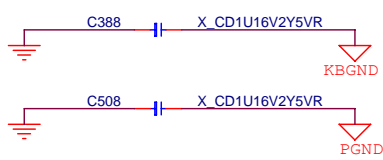
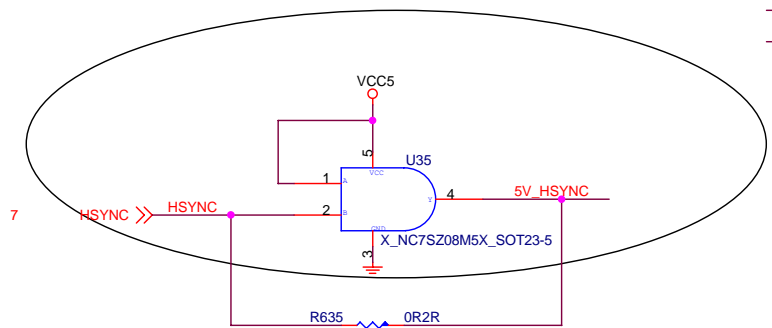
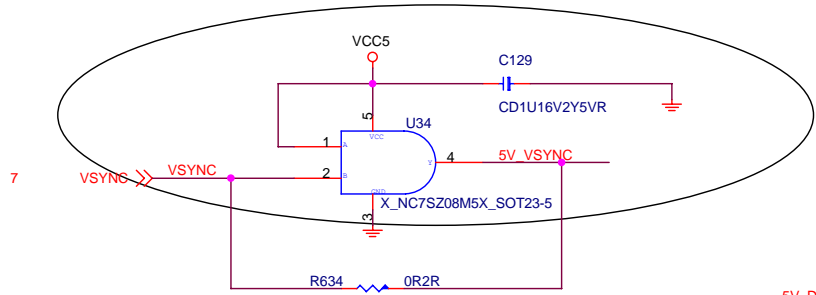
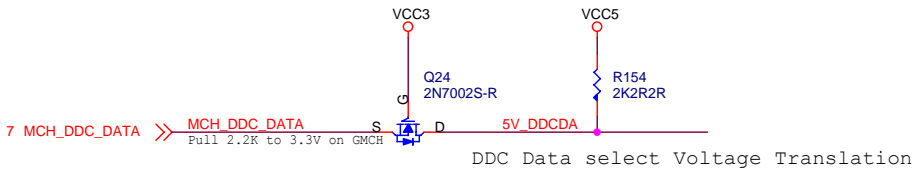
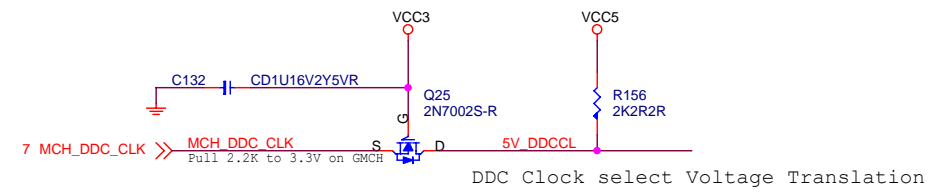












VCC3	3,4,7,9,11,12,13,14,15,16,17,18,19,20,21,22,23,27,28,30
VCC5	15,16,18,19,20,22,23,26,27,28,29,30
PGND	25,26
AGND	22,30
GND	3,4,5,6,7,8,9,10,11,12,13,14,15,16,17,18,19,20,21,22,23,25,26,27,28,29,30

for Graphic G33

**MSI**  
Link to the Future  
**MICRO-START INT'L CO.,LTD.**

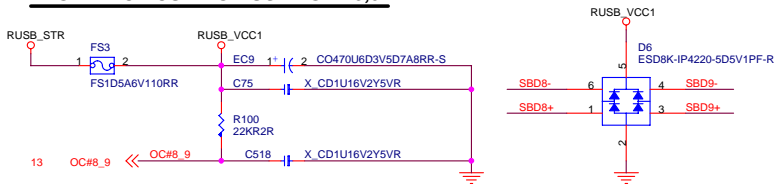
Title  
**On Board VGA Connector**

Size Custom	Document Number <b>MS-7356</b>	Rev <b>10</b>
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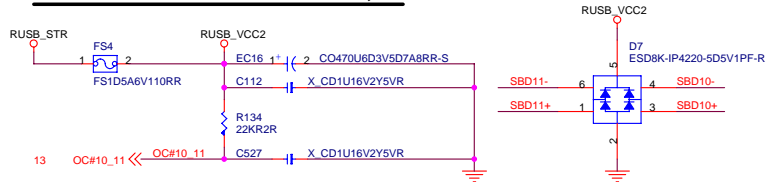
Date: Monday, April 16, 2007 Sheet 24 of 36

## Rear USB Connector

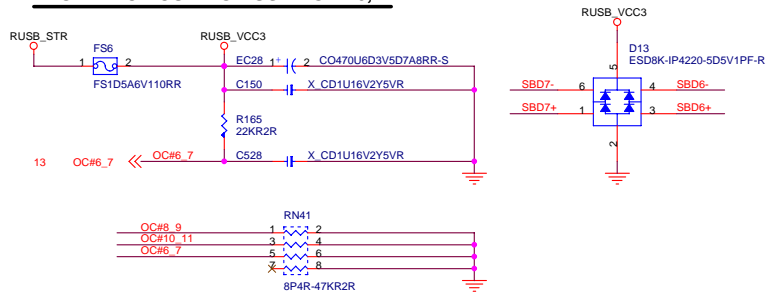
### POWER CIRCUIT FOR USB PORT 3,6



### POWER CIRCUIT FOR USB PORT 9,10

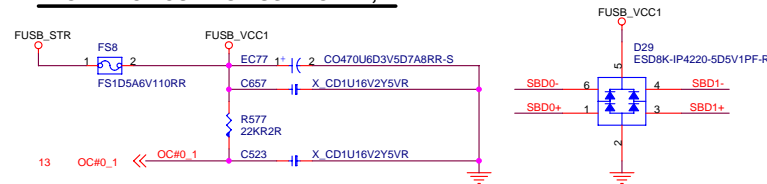


### POWER CIRCUIT FOR USB PORT 0,2

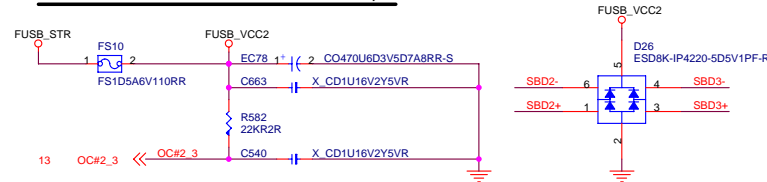


## Front USB Connector

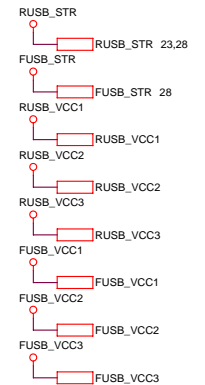
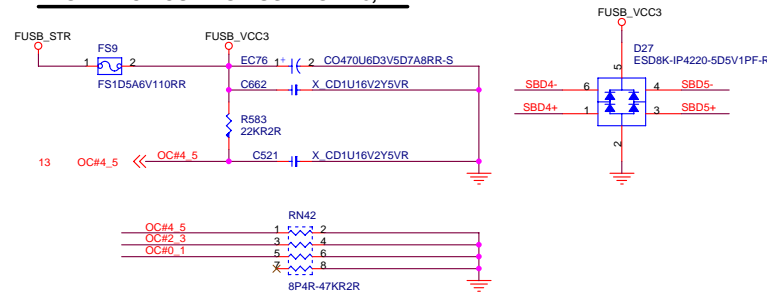
### POWER CIRCUIT FOR USB PORT 1,4



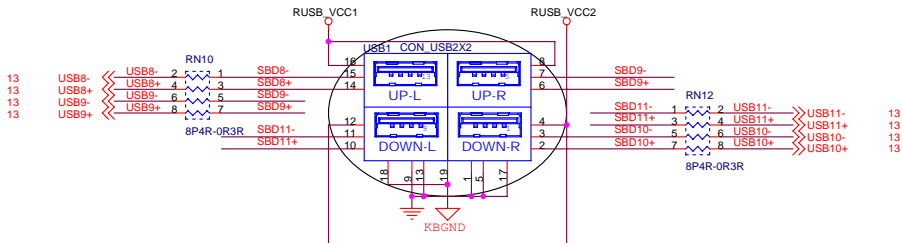
### POWER CIRCUIT FOR USB PORT 5,7



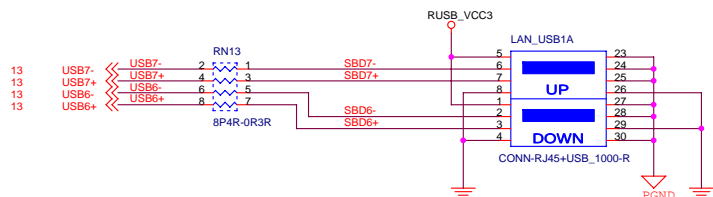
### POWER CIRCUIT FOR USB PORT 8,11



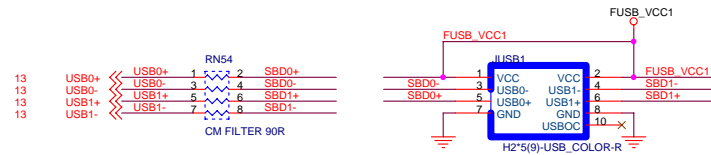
### REAR PANEL USB CONNECTOR FOR USB PORT 6,3,9,10



### REAR PANEL USB CONNECTOR FOR USB PORT 0,2



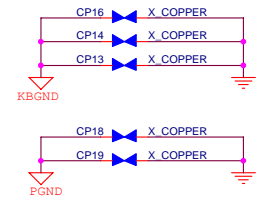
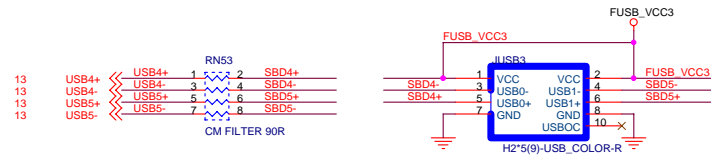
### FRONT PANEL USB CONNECTOR FOR USB PORT 1,4



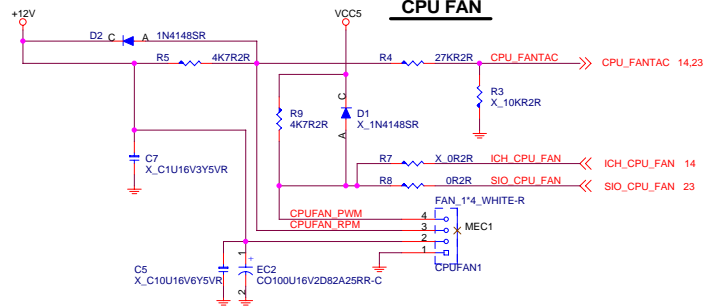
### FRONT PANEL USB CONNECTOR FOR USB PORT 5,7



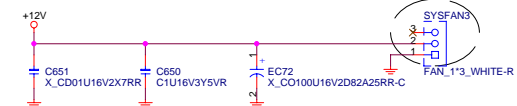
### FRONT PANEL USB CONNECTOR FOR USB PORT 8,11



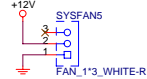
## CPU FAN



## SYSTEM FAN 3

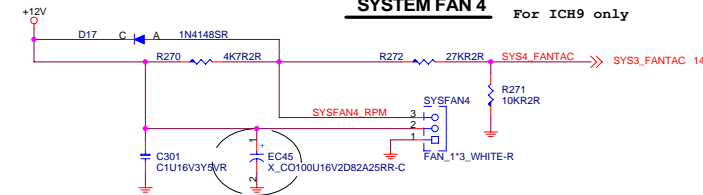


## SYSTEM FAN 5

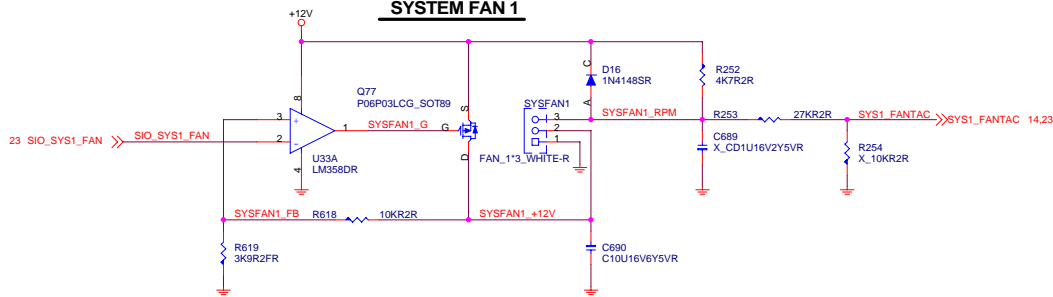


## SYSTEM FAN 4

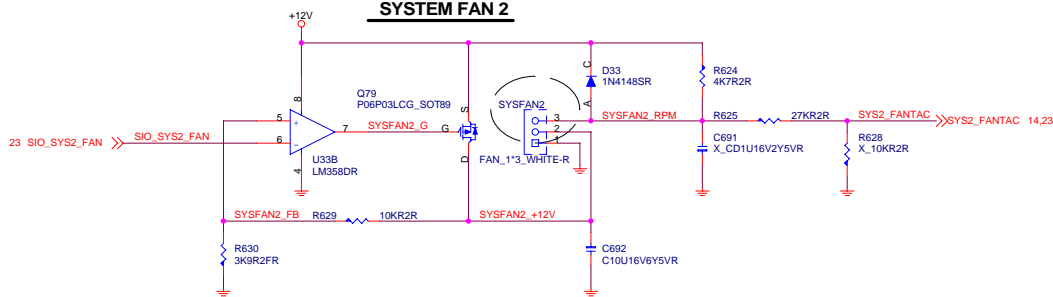
For ICH9 only



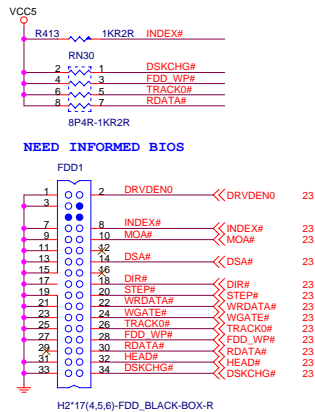
## SYSTEM FAN 1



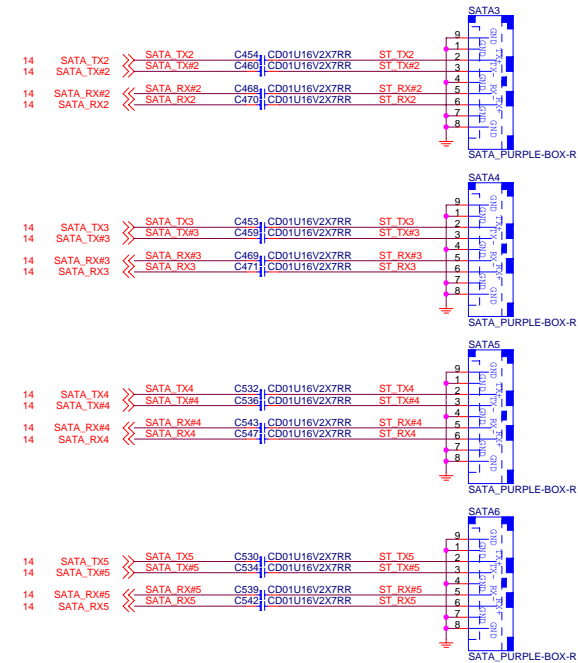
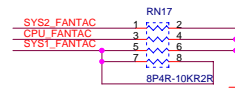
## SYSTEM FAN 2



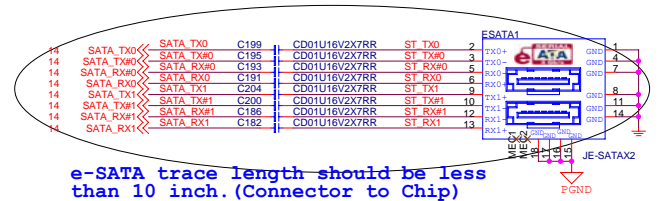
## FLOPPY CONNECTOR



Peak FAN current draw ----- 1.5A  
Average FAN current draw --- 1.1A  
Fan Start-up current draw -- 2.2A



e-SATA trace length should be less than 10 inch. (Connector to Chip)





### Reference Voltage Output

3.11,27,30 SMBCLK\_ISO >> SMBCLK\_ISO R277 22R2R SMBCLK\_REF 4

3.11,27,30 SMBDATA\_ISO R276 22R2R SMBDATA\_REF 4

29 5VDRV1 >> 5VDRV1 R287 200K REF\_ENB 8

1.8VREF

1.25VREF

1.2VREF

R298 56K2R2F

R275 10R2R

R277 22R2R

R276 22R2R

R287 200K

R298 56K2R2F

C362

C374

C383

C387

R600 11K2R2F

R620 X\_11K2R2F

uP6261B

5VSB

1.8VREF

1.25VREF

1.2VREF

5VSB

VCC5

REF\_PWR

SCL

SDA

EN

GND

DDR3 1.5V REF

NB 1.25V REF

FSBTTT 1.2V REF

\*Reference sinking/sourcing 100uA

\*Reference ramp-up 5ms

ICH GPIO2/3 for over voltage V\_1P5\_Ich

V1_5SET_0=0	V1_5SET_1=0	1.5V
V1_5SET_0=1	V1_5SET_1=0	1.6V
V1_5SET_0=0	V1_5SET_1=1	1.7V
V1_5SET_0=1	V1_5SET_1=1	1.8V

[illegible]

## 5VDUAL FOR Front USB

The diagram illustrates the 5VDUAL circuit for the front USB. The central component is the P5003QVG chip, which is connected to various power and signal lines. The connections are as follows:

- Pin 1: 5VBUS
- Pin 2: VCC5
- Pin 3: 5VDRV1
- Pin 4: 5VSDRV2
- Pin 5: 5V
- Pin 6: 5V
- Pin 7: FUSB\_STR
- Pin 8: FUSB\_STR

Additional components and connections include:

- Capacitor C624 connected between 5VSDRV2 and ground.
- Capacitor C627 connected between C627 and ground.
- Capacitor CD018U16V2X7RR connected between C627 and ground.





### ATX CONNECTOR

The diagram illustrates the ATX connector wiring for the PWR-2X12M-WHITE-R module. It shows the connection of various power rails and signals between the module's pins and external components. Key components include resistors (R186, R604, R255, R256), capacitors (C178, C181, C197, C251, C275, C264, C238), and a PS\_ON# button (RN2). The power rails shown are +5VSB, +3.3V, +5V, +12V, -5V POK, and GND. The signal ATX\_PWR\_OK is also connected to pin 22.

**H.D. LED**

VCC3

R332 4K7R2R

R542 10KR2R

20 JM\_IDELED#

14 ICH\_SATALED#

Open-collector

D21 BAT54S-R

3

C646 X\_CD1U16V2Y5VR

H.D. LED

HDDLED

### Power LED

3VSB

RN51

1 2 3 4 5

PWR\_LED# B

Q56 2N3904S-R

SWS\_LED#

SWS\_LED#

SWS\_LED#

Q58 2N3904S-R

LED VCC

LED VSB

LED VCC

LED VSB

23 23

**INTEL Front Panel**

The diagram illustrates the electrical connections for the Intel Front Panel, divided into two sections: Front Panel A-R (JFP1) and Front Panel B-R (JFP2).

**Front Panel A-R (JFP1):**

- Power Supply:** 3VSB is connected to the panel through resistor R527 (X1KR2R). 5VSB and 6VSB are connected through resistors R535 (1KR2R) and R536 (10R2R) respectively. VCC5 is connected through capacitor C647 (CD1U16V2Y5VR) and resistor RN50 (8P4R-330R3R).
- Signal Connections:**
  - HDD+ (Pin 1) and HDDLED (Pin 3) are connected to the HDD+ and HDDLED pins of JFP1.
  - RESET- (Pin 5) and R\_FPRST# (Pin 7) are connected to the RESET- and R\_FPRST# pins of JFP1.
  - NC (Pin 8) is connected to the NC pin of JFP1.
  - PLED (Pin 2) and SLED (Pin 4) are connected to the PLED and SLED pins of JFP1.
  - PWSW+ (Pin 6) and PWSW- (Pin 8) are connected to the PWSW+ and PWSW- pins of JFP1.
  - SWITCH ON# (Pin 9) is connected to the SWITCH ON# pin of JFP1.
  - PWRBTN (Pin 10) is connected to the PWRBTN pin of JFP1.
- Resistors and Capacitors:** R534 (10R2R) is connected between WDT# and WDT#. R539 (10R2R) is connected between FP\_RST# and FP\_RST#. C623 (CD1U16V2Y5VR) is connected between 3VSB and ground. C619 (C1U16V3Y5VR) is connected between 5VSB and ground.

**Front Panel B-R (JFP2):**

- Power Supply:** 5VSB is connected to the panel through resistor R535 (1KR2R). VCC5 is connected through capacitor C647 (CD1U16V2Y5VR) and resistor RN50 (8P4R-330R3R).
- Signal Connections:**
  - GND (Pin 1) and SLED (Pin 3) are connected to the GND and SLED pins of JFP2.
  - PLED (Pin 5) and BUZZER- (Pin 2) are connected to the PLED and BUZZER- pins of JFP2.
  - BUZZ+ (Pin 4) and VCCSPK (Pin 6) are connected to the BUZZ+ and VCCSPK pins of JFP2.
- Resistors and Capacitors:** R536 (10R2R) is connected between 5VSB and ground. C619 (C1U16V3Y5VR) is connected between 5VSB and ground.

**LEDs and Test Points:**

- LED19 (X\_LED\_BLUE-SR) and LED20 (X\_LED\_BLUE-SR) are connected to the PLED and SLED pins of JFP1.
- LED19 (X\_LED\_BLUE-SR) and LED20 (X\_LED\_BLUE-SR) are connected to the PLED and SLED pins of JFP2.
- Test Only: The diagram includes a note "Test Only" at the bottom left.

[illegible]

## Mounting Holes

## Simulation

## Optical Fiducial Marks-100

## Optical Fiducial Marks-100